INDEX LABS K7DYY Super Senior Circuit Walkthrough and Analysis

April 1, 2026

Introduction:

This document is intended to assist to those individuals who wish to understand the circuits, logically diagnose, quickly repair, and of course enjoy operating the Index Labs K7DYY 8040 Super Senior transmitter designed, manufactured, and supported by the late Bruce Franklin, amateur radio operator K7DYY.

A K7DYY Shortwave Broadcast Transmitter, very similar to the 8040 and 80/160 models

For basic Super Senior troubleshooting and repair, please refer to the *Index Labs K7DYY Super Senior Troubleshooting and Maintenance* PDF, available here

https://www.wirelessgirl.net/k7dyyfiles/K7DYY_Repair_Tutorial.pdf

Table Of Contents:

Documentation Strategy:

Rather extensive component-level functional detail is included, making the document rather long, so if you are simply looking for a quick guide to tell you which component to replace for a specific symptom, you may wish to look elsewhere.

The intent here is to not only assist with an understanding to enable diagnosis and repair, it is also prudent to identify and address the root cause of any failure, instead of just substituting replacement parts for those that failed as a result of some other underlying issue. In many cases where active components are directly connected in cascade, the identified failed component is often NOT the device that instigated the failure. The root cause may lie either upstream, or in some cases, downstream from the first identified failed component. Extensive analysis is recommended prior to replacing the first failed component located.

Measurements, Math, and unnecessary Engineering Details are intentionally excluded. That content is reserved for the companion troubleshooting document, which includes real-world issues and their appropriate resolutions.

It should also be stated that when dealing with the replacement of an obsolete component, a substitute may seem appropriate based upon voltage, current, and dissipation specifications, but timing, input, and output capacity are also of major importance when selecting or qualifying an appropriate substitute component.

The content is subdivided into functional blocks, enabling the reader to focus on any specific area of interest, however it follows, in general, the signal flow through the transmitter from the microphone (line level) input to the 50 ohm non-inductive output to either an external tuner or direct to an antenna system.

Other than the required difference in component values, this document "should" also be reasonably applicable to the K7DYY Super Senior 80-160 transmitter. Please refer to the schematic diagrams of that product, if they are available, to identify any differences in the design and implementation..

Informational Resources:

The sole sources of information utilized in the preparation of this document are the schematic diagrams listed below, and the individual manufacturer's component datasheets available online.

The schematic diagrams are available via links within this website.

For the complete datasheet content, please visit the manufacturer's website. Because manufacturers website content is dynamic, direct links to their resources will not be included, thus avoiding broken links. ***(See Note 1 below)

Suggested links are included in the bibliography, and will also be listed in the sections where the specific components are discussed. If the suggested links fail, search the manufacturer's site or use your preferred search engine to obtain the current datasheet information.

***Note 1:

This syndrome is analogous to trusting your GOOGLE MAP directions on your in-dash global guidance system, and getting "navigationally impaired", when the display guides you to the end of a dead-end road, and the message appears on the map display "Error 404: Road Not Found". Your webmaster takes every possible precaution to prevent you from experiencing such torturous situations! (Just checking to see if I have your undivided attention!)

Unreferenced Note 2:

In "the end", the writers CAPITALIZED on the "security" provided by intuitively obvious obfuscation.

Unreferenced Note 3:

While this document was first released on April first, 2026, the technical content is intended to be factual, and as accurate as could be determined based upon the available resources and external reference documents. If any inaccuracies are discovered, the author(s) will make an earnest attempt to make appropriate corrections to the content when such issues are reported. Contributing author(s) and editors(s) are listed immediately following the bibliography.

A word about copyright compliance

The four schematic diagrams included in this document were produced by Bruce D. Franklin, the originator and manufacturer of the K7DYY Super Senior series of Amplitude Modulated transmitters for amateur radio use. These diagrams are normally provided for each user, such that practical operation, maintenance, and when desired, modifications may be accomplished.

Several general-purpose integrated circuits and other components are included in the transmitter product. Relevant pinout reference diagrams and basic functionality descriptions of these components have been selectively included from the manufacturer's published and freely-available datasheets. None of the manufacturer's documents have been copied in their entirety. Manufacturer's produce the datasheets, not only to market their components, but also to assist and guide engineers, service representatives, and consumers in the practical application of their components.

Based upon a review of the "Fair Use Copyright Doctrine", copyright law allows limited use of copyrighted material without permission for specific purposes. The purpose of this document is purely educational, and in no way commercial. The limited use of the diagrams and reference information is common practice in the use of the associated products, and in so doing it actually provides advertising at no cost to the component manufacturer.

If at any time a concern arises with regard to the legality and the appropriate inclusion of this limited reference data, it will be promptly deleted upon request.

Reference Documents:

The K7DYY schematic diagram set is available in PDF format on the website; copies are included in this document within the relevant sections.

2015-03-22 rev 1.1 PDF 8040 Super Pan:

Front Panel Display, Microcontroller, PLL VFO, Audio Processing

2015-03-22 rev 1.2 PDF 8040 Super PWM:

Power Supplies, Optical Isolator, PWM generator, PWM Filter

2014-08-20 rev 1.0 PDF 8040 Super LPF:

Band Pass Filters, Reflected Power Detector, T/R Switching

2015-03-22 rev 1.1 PDF 8040 Super RF:

Current Mode Class-D PA with Parallel Modules, Single Coupling Transformer

Wireless Girl Website by Janis AB2RA

https://www.wirelessgirl.net/

K7DYY website by the late Bruce Franklin

http://www.k7dyy.com/

K7DYY Archive Mirror Website by Don and Janis, AC2RS, AB2RA

https://www.wirelessgirl.net/K7DYY/

Detailed Schematic Walkthrough

of the Index Labs K7DYY 8040 Super Senior

Power Supplies and Safety Information:

(MUST READ BEFORE WORKING INSIDE THE PRODUCT)

WARNING:

Before making any attempt to work within the covers of this transmitter, please understand that there are high voltages exposed that present a LIFE SAFETY HAZARD if proper precautions are not exercised.

The HIGH VOLTAGE power supplies are sourced directly from the incoming 120 volt AC Line, with no isolation. High Voltages appear on what would otherwise be assumed to be at ground potential. This should in no way be construed as a design defect or shortcoming. It is an elegant implementation which improves operational efficiency and reduces the size, weight, and cost of the product. However, since the power supply does not employ the conventional isolating power transformer, special techniques must be used in order to make internal measurements or adjustments.

Please study the schematic diagrams to familiarize yourself with the circuit operation, and if the risks are not fully understood, refer servicing to fully-qualified personnel. The authors of this document, and the providers of the web site take no responsibility for accidents, injury, or death that may occur as a result of untrained people accessing the inside circuits of this product.

Service procedures require Extreme Care when troubleshooting or measuring the higher voltage supplies, as they are "floating", not referenced to chassis ground, and therefore meter or oscilloscope ground reference leads MUST NOT be connected to the HIGH VOLTAGE negative supply rail.

The power supplies require 120 volts alternating current, at approximately 5 amperes, protected by the circuit breaker at 8 amperes to withstand turn-on surge while charging the filter capacitor bank. A standard, three terminal power input connector provides the ground, neutral, and line connections. The line is protected by the power switch/circuit breaker. In addition, a thermistor (R1) reduces the initial surge current as the capacitor bank charges.

The power supply section includes an isolated low voltage power supply module, and two high voltage power supplies implemented with discrete components.

The low voltage isolated switching supply is a Delta SADP-65KB D MPJA, providing 19 volts DC, with the negative rail referenced to chassis ground. (While the schematic indicates 15 volts output, the gate driver integrated circuits indicate 19 volts input, so the actual power supply output is unknown.)

Where lower voltages, IE 12 VDC, 8 VDC, 5 VDC, and 3.3 VDC are required, linear regulators are employed on the PC board containing the circuits utilizing these potentials.

The main high voltage supply consists of a full wave diode bridge, charging a pair of filter capacitors (C10, C11), with parallel bleeder resistors (R17, R17) On the schematic diagram, both are labeled with the same number. This bridge is fed directly from the mains line and neutral, thus the bridge output is floating; meaning that both the negative and positive output rail are elevated to a high potential above chassis ground, so care must be exercised when working with this, and the circuits powered from this source. The negative power supply output is the common return bus for all components within the PWM modulator, and the variable output of the negative supply from the PWM modulator is the negative supply rail provided to the Class-D RF amplifier. The positive rail is supplied directly to the class-D RF amplifier.

The second high voltage supply provides the floating B+ potential for the PWM generator chip. This supply consists of a diode (D1) positive and the upper left diode of the bridge rectifier (D2) between terminals 2 and 4 negative. The following components (R2, C8, C9) filter and reduce the voltage supplied to the PWM generator chip (U2). Within the PWM chip, a shunt regulator limits the voltage on VDD pin (3) to approximately 14 volts at 10 milliamperes input current. When not loaded by the shunt voltage regulator within the PWM Generator IC, (with the chip out of the circuit) the voltage will rise to approximately 25 volts DC.

Microcontroller Responsibilities:

Note: The terms Microcontroller and Processor may be used interchangeably throughout this document.

A Microchip "PIC" Microcontroller (16F872 30221c PIC)

performs the following functions:

1. Receive a single phase 8 MHz clock signal to properly time instruction stepping
2. Monitor and respond to the frequency encoder, spot and transmit/receive switches
3. Send information to be viewed on the LCD display module
4. Increment/decrement desired operating frequency
5. Send code word to PLL VFO chip SI570 (u4) such that desired frequency is generated
6. Enable/Disable PLL VFO and frequency divider flip flop (U1)
7. Output a control signal to band selection relays when transitioning between the 80 and 40 meter bands
8. Respond to SWR Latch (protection trip) signal and perform an immediate, orderly shutdown

(Note: The processor does not "decide" when to instigate a protection trip, it simply responds to the detection logic and performs the status change to shut down Transmit power output when commanded by the detection circuit).

The processor, clock oscillator, display module, and PLL VFO frequency generator (VFO) are all powered by the 3.3 volt regulator (U2). The processor ground terminals are pins (8, 19); positive 3.3 volts DC is applied to pin (20).

CAUTION: The processor (microcontroller) operates at a mere 3.3 volts, and, as such, it may receive inputs on the I/O port pins within a voltage range between zero and 3.3 volts. Applying voltages greater than 3.3 volts to any pin of the microcontroller will likely cause unrecoverable damage. Note that signals from the PTT and SWR protection trip are "LEVEL SHIFTED" from 12 volts to 3.3 volts via a pullup resistor and decoupling diode. Under no circumstances should any 5 or 12 volt signals be directly connected to the microcontroller. Some of the pins may be 5 volt "TTL Compatible", but it is prudent to consult the detailed datasheet before subjecting any of the pins to a potential greater than 3.3 volts DC.

Microchip PIC Microcontroller Reference Information:

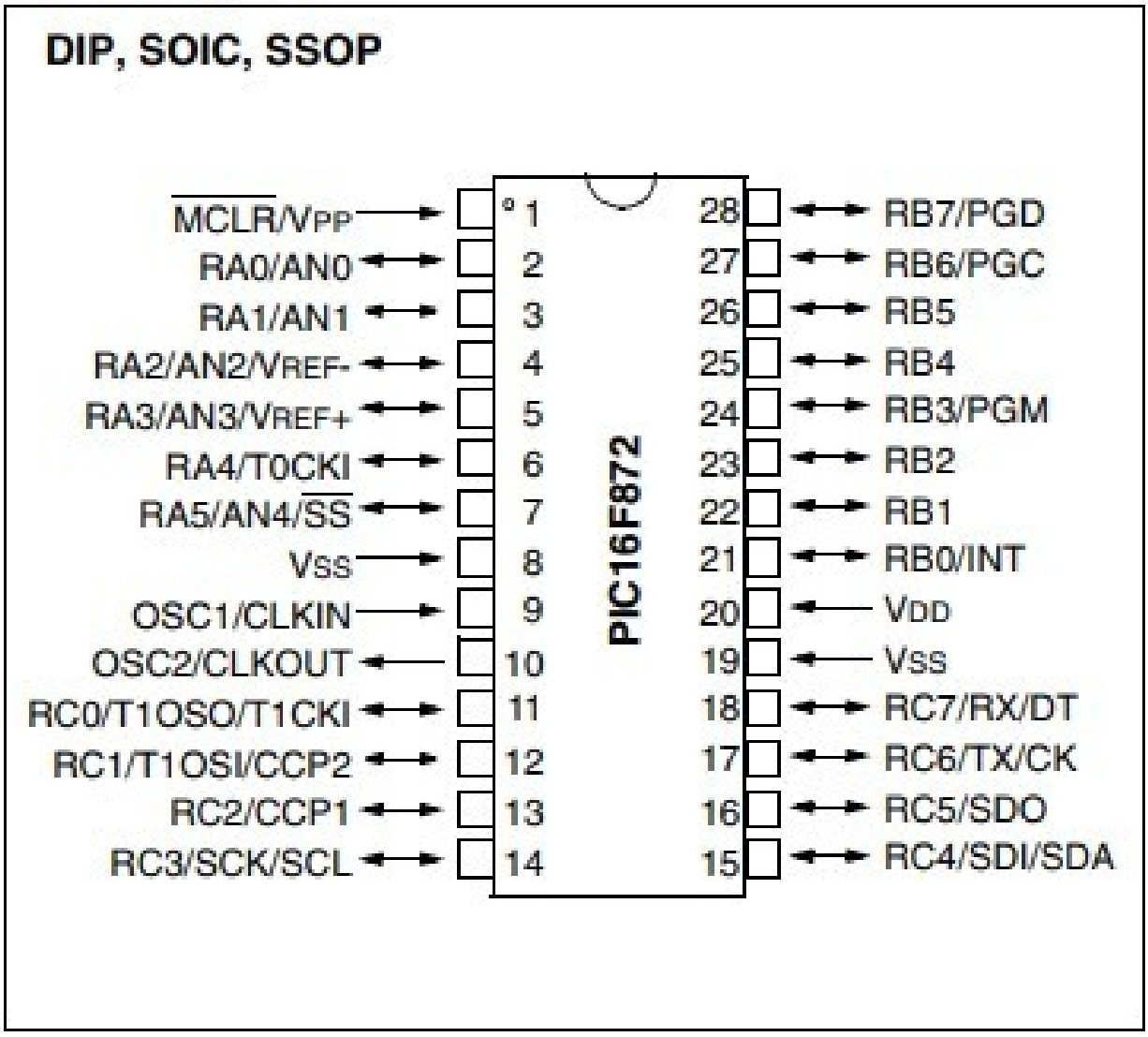
Microchip PIC16F872

28-Pin, 8-Bit CMOS FLASH Microcontroller with 10-bit A/D

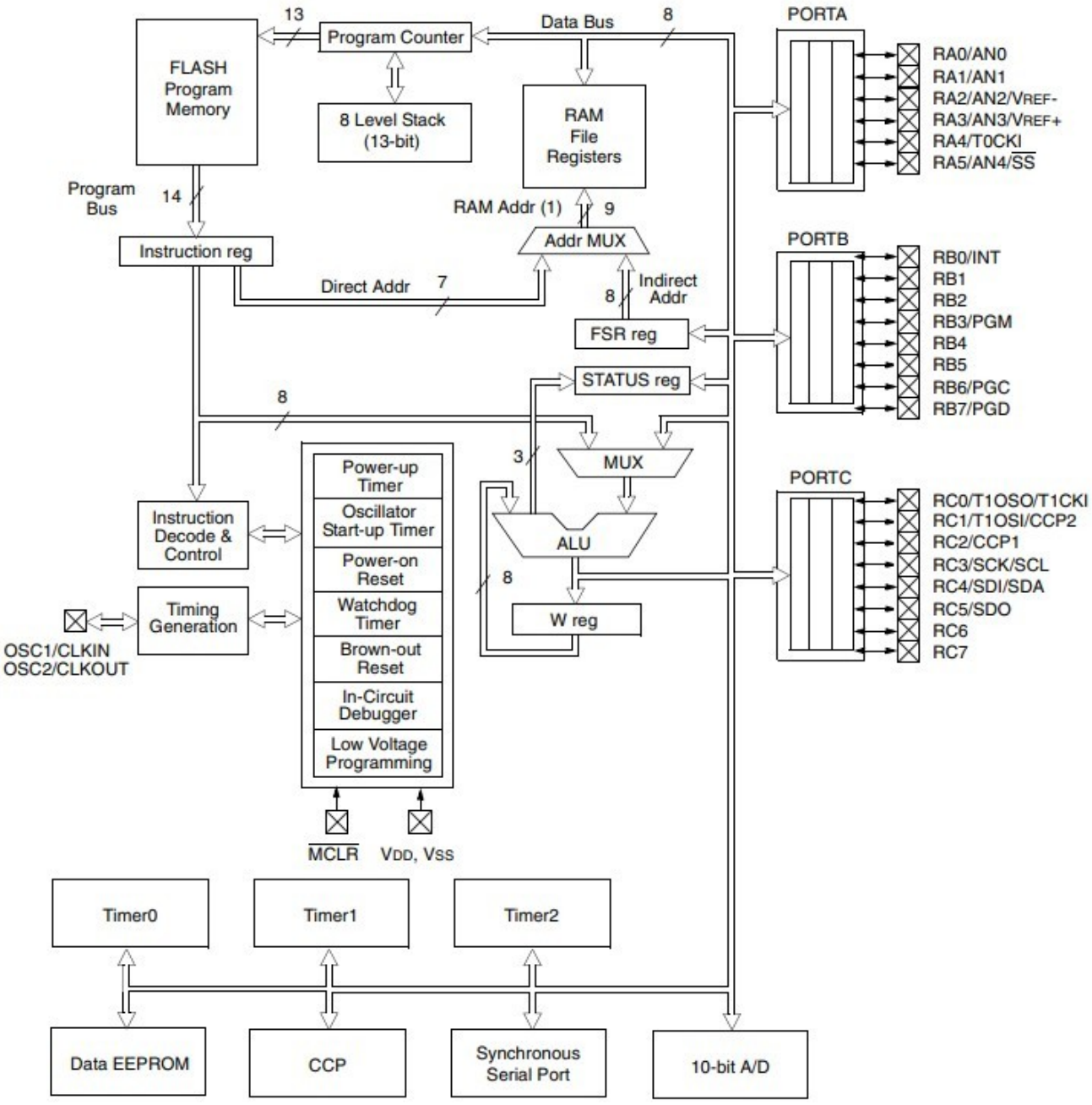
Operating Frequency	DC - 20 MHz
RESETS (and Delays)	POR, BOR (PWRT, OST)
FLASH Program Memory (14-bit words)	2K
Data Memory (bytes)	128
EEPROM Data Memory (bytes)	64
Interrupts	10
I/O Ports	Ports A, B, C
Timers	3
Capture/Compare/PWM module	1
Serial Communications	MSSP
10-bit Analog-to-Digital Module	5 input channels
Instruction Set	35 Instructions
Packaging	28-lead PDIP 28-lead SOIC 28-lead SSOP

PIC Microcontroller Key Features

Pin Diagram



PIC Microcontroller Pin Assignments



PIC Microcontroller Functional Block Diagram

TABLE 1-2: PIC16F872 PINOUT DESCRIPTION

Pin Name	Pin#	I/O/P Type	Buffer Type	Description
OSC1/CLKI OSC1 CLKI	9	I	ST/CMOS	Oscillator crystal or external clock input. Oscillator crystal input or external clock source input. ST buffer when configured in RC mode. Otherwise CMOS. External clock source input. Always associated with pin function OSC1 (see OSC2/CLKO pin).
OSC2/CLKO OSC2 CLKO	10	O	—	Oscillator crystal or clock output. Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. In RC mode, OSC2 pin outputs CLKO, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
$\overline{MCLR}$/VPP $\overline{MCLR}$ VPP	1	I/P	ST	Master Clear (input) or programming voltage (output). Master Clear (Reset) input. This pin is an active low RESET to the device. Programming voltage input.
				PORTA is a bi-directional I/O port.
RA0/AN0 RA0 AN0	2	I/O	TTL	 Digital I/O. Analog input 0.
RA1/AN1 RA1 AN1	3	I/O	TTL	 Digital I/O. Analog input 1.
RA2/AN2/VREF- RA2 AN2 VREF-	4	I/O	TTL	 Digital I/O. Analog input 2. Negative analog reference voltage.
RA3/AN3/VREF+ RA3 AN3 VREF+	5	I/O	TTL	 Digital I/O. Analog input 3. Positive analog reference voltage.
RA4/T0CKI RA4 T0CKI	6	I/O	ST	 Digital I/O; open drain when configured as output. Timer0 clock input.
RA5/$\overline{SS}$/AN4 RA5 $\overline{SS}$ AN4	7	I/O	TTL	 Digital I/O. Slave Select for the Synchronous Serial Port. Analog input 4.

Legend: I = input O = output I/O = input/output P = power
— = Not used TTL = TTL input ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.
2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.

PIC Microcontroller Pinout Description Page 1 of 2

				PORTB is a bi-directional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs.
RB0/INT	21	I/O	TTL/ST(1)	
RB0				Digital I/O.
INT				External interrupt pin.
RB1	22	I/O	TTL	Digital I/O.
RB2	23	I/O	TTL	Digital I/O.
RB3/PGM	24	I/O	TTL	
RB3				Digital I/O.
PGM				Low voltage ICSP programming enable pin.
RB4	25	I/O	TTL	Digital I/O.
RB5	26	I/O	TTL	Digital I/O.
RB6/PGC	27	I/O	TTL/ST(2)	
RB6				Digital I/O.
PGC				In-Circuit Debugger and ICSP programming clock.
RB7/PGD	28	I/O	TTL/ST(2)	
RB7				Digital I/O.
PGD				In-Circuit Debugger and ICSP programming data.
				PORTC is a bi-directional I/O port.
RC0/T1OSO/T1CKI	11	I/O	ST	
RC0				Digital I/O.
T1OSO				Timer1 oscillator output.
T1CKI				Timer1 clock input.
RC1/T1OSI	12	I/O	ST	
RC1				Digital I/O.
T1OSI				Timer1 oscillator input.
RC2/CCP1	13	I/O	ST	
RC2				Digital I/O.
CCP1				Capture1 input/Compare1 output/PWM1 output.
RC3/SCK/SCL	14	I/O	ST	
RC3				Digital I/O.
SCK				Synchronous serial clock input/output for SPI mode.
SCL				Synchronous serial clock input/output for I^2C mode.
RC4/SDI/SDA	15	I/O	ST	
RC4				Digital I/O.
SDI				SPI Data In pin (SPI mode).
SDA				SPI Data I/O pin (I^2C mode).
RC5/SDO	16	I/O	ST	
RC5				Digital I/O.
SDO				SPI Data Out pin (SPI mode).
RC6	17	I/O	ST	Digital I/O.
RC7	18	I/O	ST	Digital I/O.
VSS	8, 19	P	—	Ground reference for logic and I/O pins.
VDD	20	P	—	Positive supply for logic and I/O pins.

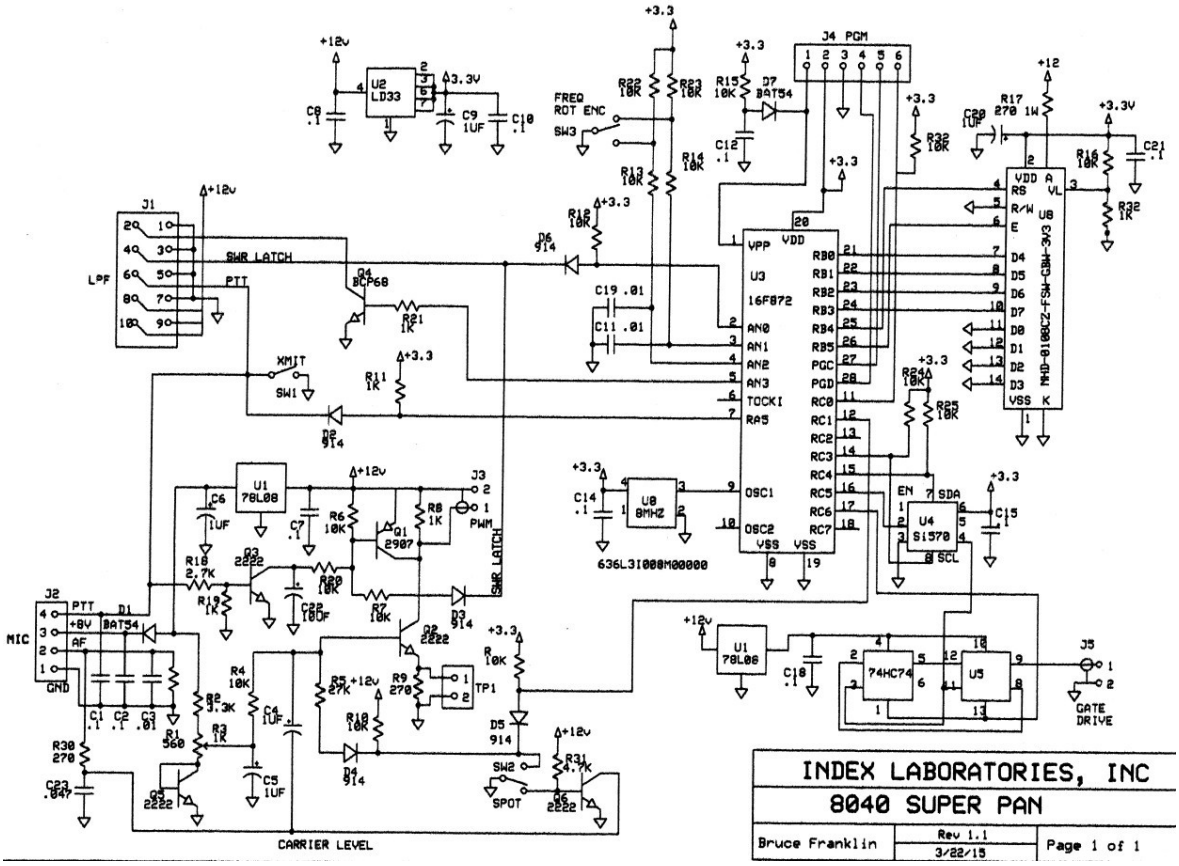
Legend: I = input O = output I/O = input/output P = power
— = Not used TTL = TTL input ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.
2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.

PIC

PIC Microcontroller Pinout Description Page 2 of 2

Upon initial power-up, the microcontroller requires a positive-going signal on the reset pin (1) after power supply voltage has stabilized. To ensure an orderly startup occurs, a time constant set by charging capacitor (C12) through resistor (R15) applies this positive-going potential to reset pin (1) via isolation diode (D7). The microcontroller performs the initial "setup" logic instructions, then executes the main "loop" function code continuously, until power is removed.



Schematic Diagram: K7DYY 8040 Super PAN

Microcontroller and Front Panel Logic

Datasheet links to components used in the microcontroller and front panel assembly:

16F872 Microchip "PIC" Microcontroller: 30221cPIC

https://ww1.microchip.com/downloads/en/DeviceDoc/30221c.pdf

CTS Model 636 HCMOS Clock Oscillator: clock-ocillators-636-datasheet

https://www.ctscorp.com/Files/DataSheets/Passives/FCP/Clock-Oscillators/clock-ocillators-636-datasheet.pdf)

Liquid Crystal Data Display: NHD-0108CZ

https://newhavendisplay.com/content/specs/NHD-0108CZ-FL-GBW.pdf

SI570 PLL VFO: si570

https://www.mouser.com/catalog/specsheets/si570-571.pdf

74HC74 Flip Flop: 74HC74

https://www.mouser.com/datasheet/2/308/74HC74-108792.pdf

Typical Microcontroller Functions, Capabilities, and Interfaces:

The processor has an eight-bit bus, and three separate 8 bit I/O ports (A, B and C), however it is common practice to utilize the pins of the I/O ports individually, reading inputs and controlling output devices with a single wire. Input and output ports may be digital (binary), acting on a single on or off, zero or one status, which may be either a low or high voltage (0 or <3.3 volts); the pins might be analog, measuring a voltage with an internal analog to digital (ADC) converter; or output a variable voltage converting a register value to a specific voltage level via an internal pulse width modulator (PWM), the output of which may be filtered to pure DC outside the processor.

Certain pins may also be used to process an interrupt", such that program flow is redirected to the address of an interrupt service routine (ISR) to deal with a high priority event, after which the interrupt service routine is exited, and normal program flow is resumed where it left off. Several or all pins within an eight-bit port may also be read or written as a group, simultaneously, as required by the specific application to be performed. Operating modes for each pin, or group of pins, are defined, or "SET" within the initialization setup loop. or may be changed anywhere within the main processing loop. Some pins include a software-enabled pull-up resistor, making it unnecessary to add external resistors to provide this function on tri-state inputs and outputs. The range of capabilities of each individual pin are clearly specified in the datasheet link for the Microchip PIC.

Programming Microcontroller Flash Memory:

The program that guides the microcontroller to perform the desired tasks is deposited into the FLASH ROM memory within the PIC integrated circuit chip. This is normally done before the chip is inserted into the product, but if updates are required during the life of the product, it is beneficial to provide an interface whereby the PIC may be reprogrammed while it remains in the product. This feature is essential when the device is the SMD version, or if the through-hole pin chip is not socketed. For this purpose, connector PGM (4) is provided. This connector exposes the ground, power, reset, and three other signals to enable the programming function. These are PGC (27), PGD (28), and RC0 (11).

A few cautionary notes are relevant with regard to reprogramming the PIC. According to the manufacture's data, this device is considered "Very Secure". This means that it is virtually impossible to extract a copy of the code that was written to the flash memory. The reason it is secured is to prevent unauthorized duplication of proprietary property or intelligence, thus eliminating the undesired practice of unauthorized cloning of the device. The code may be rewritten, but any time the code is written, the original code is eradicated in its entirety.

You MUST have a copy of either compliable source code, or the binary object code file, in order to successfully update or rewrite the flash program memory content. Of course, it is possible, when designing the PIC code, to add a routine which allows the user to read the code and output it to specific output port pins, but this is normally not done, and to do so would consume precious memory, reducing the space available for the desired program to perform all the intended functions. If no known-working copy of the code for this product is immediately available, no attempt should be made to write to, or update, the flash memory contained within the PIC chip.

Some additional notes from the Microchip datasheet regarding code security, and the ability to extract a copy of the code from a programmed microcontroller device:

Microchip products meet the specification contained in their particular Microchip Data Sheet.

Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.

There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.

Microchip is willing to work with the customer who is concerned about the integrity of their code.

Operation While Code Protected:

The PIC16F872 has two code protect mechanisms, one bit for EEPROM Data memory and two bits for FLASH Program memory. Data can be read and written to the EEPROM Data memory regardless of the state of the code protection bit, CPD. When code protection is enabled, CPD cleared, external access via ICSP is disabled regardless of the state of the program memory code protect bits. This prevents the contents of EEPROM Data memory from being read out of the device. The state of the program memory code-protect bits, CP0 and CP1, do not affect the execution of instructions out of program memory. The PIC16F872 can always read the values in program memory, regardless of the state of the code protect bits. However, the state of the code protect bits and the WRT bit will have different effects on writing to program memory. Table 4-1 shows the effect of the code protect bits and the WRT bit on program memory. Once code protection has been enabled for either EEPROM Data memory or FLASH Program memory, only a full erase of the entire device will disable code protection.

FLASH Program Memory Write Protection:

The configuration word contains a bit that write-protects the FLASH Program memory called WRT. This bit can only be accessed when programming the device via ICSP (In Circuit Serial Programming) interface, IE, the PGM header at connector J4 on the K7DYY 8040 Super Pan PC Board.

Once write protection is enabled, only an erase of the entire device will disable it. When enabled, write protection prevents any writes to FLASH Program memory. Write protection does not affect program memory reads.

Perhaps, when the PICs were programmed by Bruce, K7DYY, the protection bits may not have been set, which would make it a trivial operation to read and file the binary code, using the ICSP programming port provided on the 8040 Super Senior Front Panel PCB.

The extracted file could then be used to deposit the original code into another new chip, to maintain a support inventory to service failed units.

16F872 Microchip "PIC" Microcontroller: 30221cPIC

https://ww1.microchip.com/downloads/en/DeviceDoc/30221c.pdf

Microcontroller Clock Oscillator:

The processor timing is controlled by the CTS Model 636 HCMOS Clock Oscillator (u8),

This device is powered by the 3.3 volt DC regulator on pin (4), with bypass capacitor (C14).

Output is taken from pin (3) and applied to processor pin (9).

Description

CTS Model 636 is a low cost, ultra-low voltage clock oscillator supporting HCMOS output. Employing the latest IC technology, M636 has excellent stability and low phase jitter performance.

Model 636 HCMOS Clock Oscillator Features

♣ Ceramic Surface Mount Package

♣ Operating Temperature Range to -40°C to +105°C

♣ Fundamental and 3rd Overtone Crystal Designs

♣ Frequency Range 1.0 – 160MHz

♣ +1.8V, +2.5V, +3.3V and +5.0V Operation

♣ Output Enable Standard

♣ Tape and Reel Packaging, EIA-481

Pin Assignments

Pin	Symbol	Function
1	EOH	Enable
2	GND	Circuit & Package Ground
3	Output	RF Output
4	V_{CC}	Supply Voltage

(https://www.ti.com/lit/ds/symlink/ucc35702.pdf?ts=1774145062177)

CTS Model 636 HCMOS Clock Oscillator: clock-ocillators-636-datasheet:

LCD Display Interface:

Frequency and status information are displayed on the one-line, eight-character display, part number NHD-0108CZ-FSW-GBW-33V3.

If one studies the schematic diagram, it is apparent that all input/output pins of each I/O port A, B and C are used individually, with the exception of four pins which send data to the LCD display module. Characters to be displayed are sent in two separate cycles, thus enabling the display to receive characters encoded in eight bits. Four bits at a time are sent from processor ports RB0, RB1, RB2, and RB3, pins (21, 22, 23, 24) to the data port of the display module, while ports RB4 and RB5, pins (25, 26) are used to select the desired register and enable the data to be transferred into the display memory. While custom character sets may be programmed on the LCD display, the processor utilizes the built-in character set, by sending the relevant ASCII value to the display module for each character position. A cursor position may be set, such that a portion of the display may be updated, without the need to rewrite the entire array of display data.

Data is sent to the display four bits at a time, on the display module lines D4, D5, D6, and D7, pins (7, 8, 9, 10). The other four bits, D0, D1, D2, D3, pins (11, 12, 13, 14) used only for eight-bit transfers, are not connected. When writing commands or data characters to the display, register select RS, pin (4) selects whether the bits transferred are to be interpreted as configuration register update parameters, or data to be stored in memory to be displayed as a combination of illuminated pixels representing a visible character. When accessing the parameter register files, the display is initialized to utilize four-bit, instead of eight-bit communications, among other things. When writing to the device, the transfer is processed when a strobe pulse is received on the enable line E, pin (6).

Since it is only desired to write to the display, but not read the display memory, the Read/Write R/W pin (5) is permanently tied low, allowing only write access mode.

Power (3.3 VDC) is applied to the display on pin (2), and is bypassed by capacitor (C20). Ground for the display logic is pin (1).

The display contrast is set by the voltage on VL, pin (3); the value is determined by voltage divider (R16, R32). If the contrast voltage is not correct, either it will be difficult to see any character pixels, or the background will be darker and boxed-in within the area of the pixels at each character position.

In order to provide the necessary backlight, the LED cathode is grounded at pin (K), and the required positive voltage is applied to the anode, pin (A), through dropping resistor (R17) which determines the brightness of the backlight. If there is no backlight, measure voltage at (K), or measure the resistor (R17).

Pin Description

Pin No.	Symbol	External Connection	Function Description
1	V_{SS}	Power Supply	Ground
2	V_{DD}	Power Supply	Supply Voltage for logic (+5.0V)
3	V_0	Adj Power Supply	Supply Voltage for contrast (approx. 0.6V)
4	RS	MPU	Register Select signal. RS=0: Command, RS=1: Data
5	R/W	MPU	Read/Write select signal, R/W=1: Read R/W: =0: Write
6	E	MPU	Operation Enable signal. Falling edge triggered.
7-10	DB4 – DB7	MPU	Four high order bi-directional three-state data bus lines.
11-14	DB0 – DB3	MPU	Four low order bi-directional three-state data bus lines. These four are not used during 4-bit operation.
A	LED+	Power Supply	Backlight Anode (+4.0V)
K	LED-	Power Supply	Backlight Cathode (Ground)

PIN ASSIGNMENT

1	VSS
2	VDD
3	V0
4	RS
5	R/W
6	E
7~10	DB4~DB7
11~14	DB0~DB3
A	LED+
K	LED-

Liquid Crystal Data Display: NHD-0108CZ

https://newhavendisplay.com/content/specs/NHD-0108CZ-FL-GBW.pdf

Rotary Encoder:

The rotary encoder is the knob interface the operator uses to raise or lower the operating frequency. It looks similar to a potentiometer, with a rotating shaft and three terminals, but internally it is a pair of switches, which are individually turned on and off as the shaft rotates. The switches and cam mechanism are designed such that when turning in one direction, switch A closes and opens before switch B, and when turning in the other direction, switch B closes and opens before switch A. The timing of the opening and closing of the switch pair overlaps. If the status of both switches is presented to the microcontroller, by comparing the switch close and open relative timing of each switch, the program code may easily determine in which direction the shaft is turned, and based upon the number of open and close transitions, it can determine how far the knob is turned. Therefore the processor can determine whether to increase or decrease VFO frequency, as well as the magnitude of the change. This is referred to as "gray scale" code, and is used for almost all rotary knobs connected to any sort of processor. Encoders may use mechanical switches or optical isolators with a slotted wheel breaking the photon beam.

The two sets of switch contacts of rotary encoder (SW3) alternately ground the junctions of two resistive voltage dividers, consisting of (R22, R13, and R23, R14), altering the voltage at processor input signals AN1 and AN2. The signals are filtered by capacitors (C19 and C20), which allow only one transition in signal status per switch action, preventing "switch bounce" from creating multiple impulses from corrupting the input as the switch contacts settle after each break-to-make switch transition.

Because we do not have access to examine the source code of the rotary encoder logic in the PIC program, we must draw some assumptions. The voltage divider, sourced by the 3.3 volt regulated DC supply, will provide HALF the supply voltage, or 1.65 volts when the switch is open, and very close to zero volts when the switch is closed. Referring to the port AN1 and AN2 capabilities in the PIC datasheet, each of these inputs may function as either a digital or an analog input. This means, in digital mode, a very low voltage is a zero bit, and a voltage at least half the supply voltage is a one bit. In analog mode, an Analog to Digital Converter, or ADC, within the PIC, converts the input voltage to a binary value, based upon the default reference voltage of 3.3 volts, and the number of resolution bits (ten, in this case) provided by the ADC. Without going into further detail, it is obvious that either analog or digital input will enable the code to determine direction and distance moved, such that frequency may be incremented or decremented. According to the 8040 documentation, turning the knob faster causes a greater change in frequency for each instance of switch status change, such that moving a good distance up or down the band takes less "twist of the wrist". Turning the knob slowly allows the normal

increment of 1 KHz steps to be managed with ease. The program code in the PIC determines the delay between switch status transitions, and applies a multiplier to the delta frequency when the delay is less than the expected threshold for normal fine-tuning operations. While earlier Super Senior products provided only 5 KHz steps in frequency with the discrete component VFO, the Si50 PLL, as coded, provides 1 KHz tuning steps. While this would be insufficient for SSB or some other modes, the frequency will never need to be more than 500 Hz away from the net frequency, so this increment is considered to be sufficient resolution for AM operation.

The last tuned frequency is maintained in memory, and when the knob is turned, the value is increased or decreased, and this information is passed to the VFO section as the PIC program code follows the endless loop of all the required tasks. One thing we can determine with certainty, is that the encoder is not functioning in "interrupt mode", as the pins to which it is connected do not provide any ability to process an interrupt signal.

Also, according to the 8040 operating instructions, when the product is in "transmit mode", the encoder is disabled; that is to say that if the knob is rotated and the bit values on PIC inputs AN1 and AN3 switch on and off, this change in status is ignored by the PIC program code until the product reverts back to "receive mode".

Band Switching Detection:

There is no band switch, per se, on the control panel of the processor. Instead, the PIC program code monitors changes in frequency as the encoder knob is rotated. When tuning up from the middle of the 75 meter band, once the frequency boundary of 4.0 MHz is exceeded, the display reverts to the beginning of the 40 meter phone band.

At that point, when the display is in the vicinity of 7.1 MHz, the output of PIC port AN3, pin (5) changes state. While the transmitter was operating in the 75 meter band, the two band select relays on the Low Pass Filter board were energized, by the conducting transistor (Q4) selecting the 75 meter filter network. The PIC input to the base of transistor (Q4) now changes from a high to a low state, causing transistor (Q4) to stop conducting, so the signal passed to the band select relays via a path through (J1 pin 2) deenergizes the relays, thus enabling the 40 meter bandpass filters. In summary, the selection of the proper bandpass filter is automatically completed when the PIC determines the operator has changed the frequency from one band to the other.

Hot-switching of the relays is prevented, because the PIC code ignores any request to change the carrier frequency when in transmit mode.

Transmit Receive Switching

Transition from receive mode to transmit mode involves pulling down the PTT line from + 12 VDC to zero volts with a switch. The 12 volt bias source is the 12 volt regulated supply applied to the T/R relay coils on the LPF (low pass filter) board. Grounding the PTT line, the other side of the relay coil, energizes the relays and transitions from receive to transmit mode. More will be discussed about the relays in the LPF section.

While the 12 volts on the PTT line may be used as a signal to external circuits for control purposes, placing a current load on this line will energize the relays prematurely, so no low-impedance, or current requiring load may be placed directly on the PTT bus.

The PTT bus is accessible at J2 pin (1) of the microphone connector, J1 Pin (6) of the interconnect bus, and J4 pin (2) on the back panel accessory connector. The transition to transmit mode may be initiated by pulling any of these points to ground potential. Three practical options exist:

1) The PTT button on the external microphone

2) The front panel send/receive transmit switch

3) An external sequencer or switch via the J4 back panel accessory jack pin (6).

Asserting ground on the PTT bus causes the T/R relays to energize, connecting the transmitter output to the antenna (also disconnecting the receiver from the antenna) and providing a normally-open, common, and normally-closed set of relay contacts for any use the operator deems necessary.

The grounding of the PTT line also informs the microcontroller that transmit mode is now active as follows:

* Microcontroller pin RA5 is the T/R input port. It is normally pulled high by pull-up resistor (R11) 1 Kohm, and the pullup is tied to the 3.3 volt supply, the highest level the processor port can withstand.

* Diode (D2), a 1N914, is connected between the PTT bus and the processor T/R switching input port. When the PTT bus is pulled low, the diode conducts, reducing the PTT input port from logic 1 (3.3 volts)

to logic 0 (zero volts) and the processor polling code acts on the level change and addresses all the functions needed to switch into transmit mode. However, when the PTT bus is high (12 volts) Diode (D2) isolates the PTT line from the PIC port input RA5, preventing the 12 volt signal from damaging the microcontroller port interface.

* Additionally, the base of Q3 is pulled low, causing it to no longer conduct. To be discussed in detail later, this transistor ensures the PWM modulator is disabled, producing no output power to the class-D RF amplifier during receive mode.

When in transmit mode, the output from the PWM modulator is enabled, providing carrier level power to the final amplifier. This transition is accomplished in the following manner: Resistor (R6) 10 Kohms from positive 12 volts to the base of transistor Q1 PNP 2N2907 ensures there is no negative forward bias on the emitter base junction, as the emitter is also tied to the + 12 volt supply rail. In this state, the transistor does not conduct, therefore it allows normal output of audio and power control signals to be developed across Q2 collector load resistor (R8) 1 KOhm. The push-to-talk bus is normally at a potential of positive 12 volts due to the supply connected to each transmit receive relay coil. This bias is applied to the base of Q3 NPN 2N2222 via resistive voltage divider (R18) 2.7 Kohm and (R19) 1 KOhm, causing it to conduct. Current through the two resistors in series between the collector and the 12 volt supply rail (R20) and (R6) cause a "less positive" bias to be applied to the base of transistor Q1, causing it to conduct, thereby shunting the output of audio amplifier transistor Q2 NPN 2N2222, thus removing the signal to the optical isolator, and disabling the PWM modulator controller chip from producing any output. When the PTT line is pulled to ground during transmit mode, Q3 is biased to cutoff, therefore no bis is produced across (R6), Q1 no longer conducts, and the output of Q2 is passed to the optical isolator, providing normal carrier level bias and unrestricted audio.

Notice the shield conductor of this coaxial cable from Q2 collector and load resistor (R8) is tied to the positive 12 volt supply rail, not ground. This effectively cancels the phase inversion that would otherwise be incurred in a grounded-base amplifier stage. As the voltage on the base of Q1 becomes more positive, commanding more output voltage from the PWM generator and modulator, the voltage across R8 also rises. But the voltage between Q1 collector and ground diminishes. Therefore, by taking the signal between the collector terminal and the positive supply rail, the drive signal passed to the optical coupler on the PWM PC board rises in magnitude in step with the signal applied to the base of Q1.

The microcontroller enables the SI570 VFO to produce the desired carrier frequency, and the 74HC74 dual D flip-flop square wave buffer/frequency divider (U5) is enabled, providing a pulse train such that the class-D RF amplifier has input drive and may produce output power.

Receiver Muting:

An auxiliary transmit/receive relay is implemented on the 8040 Super LPF PCB. It operates in parallel with the antenna changeover relay coil. Both normally open and normally closed contacts are available to mute various receivers, or control other devices when transitioning between receive and transmit modes.

According to the rev 1.0 LPF schematic sheet dated 08/20/2014, the pinout is as follows:

J4 pin (3) Normally-closed during receive

J4 pin (4) Common relay terminal

J4 pin (5) Normally-open during receive, closed on transmit

Use caution before connecting any active circuits to these pins. If your 8040 transmitter complies with the referenced schematic diagram, there should be no issues. However, it has been reported that earlier cases, when using these terminals on J4, the microcontroller was damaged, indicating that on some earlier units, these pins may interface directly to microcontroller I/O port pins. Carefully testing with an ohmmeter, while switching between receive and transmit modes, should clarify whether your specific unit uses the relay contact circuit defined in the referenced schematic diagram.

Microphone Input Circuit:

Microphone input is accomplished via front panel connector J2, with microphone audio input on pin (2) referenced to ground pin (1). A push to talk switch may optionally be included in the microphone, connecting the PTT line on pin (4) to ground pin (1). Microphone input is line level, at 0 dBm into 600 ohms, which equates to 774 millivolts, or approximately 3/4 volt RMS. The microphone requires a preamplifier or processor, such as the D-104 MK2 DYY processor, which includes a phase rotator, compressor limiter, and output stage to drive the microphone cable to the low impedance unbalanced microphone input of the 8040 Super Senior Transmitter. To provide power for the processor or microphone preamplifier, which is typically installed in the base of an Astatic D-104 microphone stand, regulated positive 8 volts DC is provided on J2 pin (3) by 78L08 regulator U1. This regulator is also used to set the RF output power level control line. The 8 volt output at the microphone is protected from reverse polarity or other power source by a BAT54 diode isolating the connector from the regulator output terminal.

All three non-grounded terminals of the microphone connector are bypassed to ground, preventing RFI ingress, pin 2 (audio input) by a .01 uF capacitor (c3) and a 560 ohm resistor (R1); while the (+8 volt output and Push-To-Talk), pins 3 and 4, respectively, are bypassed by .1 uF disk ceramic capacitors. Additional RFI suppression and high frequency rolloff is provided by series resistor (R30) 279 ohms, and shunt capacitor (C23) .047 uF. Audio input is then coupled to the base of audio preamplifier transistor Q2 by 1 uF capacitor C4. transistor output is developed across collector resistor (R8) 1Kohm, and this signal is passed via coaxial cable to the linear mode optical isolator to provide both audio and power level control bias to the PWM generator chip U2.

The emitter resistor for 2N2222 Q2 is (R9) 270 ohms, and a two-pin test point header "TP1" is provided in parallel with the resistor. It is obvious that the voltage drop across the emitter resistor will increase as the power level trim pot (R3) is advanced, and the input audio signal may be sampled at this test point. However, the expected bias and signal levels, as well as the intended purpose of the test point, are currently unknown.

Power Output Control Logic:

Power output control is managed by adding a positive DC offset bias to the audio signal connected to the optical isolator which couples audio to the PWM generator chip. The optical isolator is required because the PWM generator circuit is not referenced to chassis ground, rather, it is referenced to the negative side of the non-isolated high voltage supply, the output of which is modulated and passed on to the class-D RF power amplifier.

Eight-volt regulator 78L08 U1 output provides power to the microphone processor, and is also used to set the required bias to define the desired RF output power level. This eight-volt potential is applied to a voltage divider string consisting of (R2) 3.3 Kohms, (R3) 1kohm power set trim pot (screwdriver adjusted via opening in front panel) and diode-connected transistor (Q5) 2N2222. The saturated emitter-base junction of (Q5) sets the lower limit, and the 3.3 Kohm resistor (R2) limits the upper level of the power control bias applied to the base of (Q2) via (R4). The adjustable output of trim pot (R2) is stabilized by capacitor (C5) 1 uF, and coupled to the base of the first audio amplifier transistor (Q2) 2n2222.

The combined power control bias and amplified microphone audio appear on the (Q2) collector resistor (R8) 1Kohm, and this signal is passed to the linear mode optical isolator on the PWM modulator board. The relative brilliance of the LED in the isolator sets the power level via a varying voltage on the emitter follower resistor connected to the isolator, and the audio plus the bias controls both the PWM average output (carrier level voltage, and the audio positive and negative peaks that modulate the Class-D final RF amplifier.

The maximum positive peak level applied to the PWM Generator is further limited by adjustable resistor (R20) 1 Kohms in series with the emitter follower load resistor (R8) 1 Kohms.

While the Transmit Receive transition logic, and the SWR Latch response functionality will be described in detail, it should be mentioned that Transistor (Q1) 2N2907, in parallel with collector resistor of Q2, is normally conducting in receive mode, due to the bias from (Q3) 2N2222, coupled to the base of Q1 by resistor (R20) 10 Kohms. This circuit nullifies the output power set bias provided by variable resistor (R3) until switching to transmit mode.

In a similar manner, the SWR Latch fault condition line (described in more detail later) also toggles the bias on transistor (Q1) base as follows. During normal operation, the SWR latch circuit is idle; the SWR Latch signal being active low is at about 12 volts DC when no fault is detected. Upon a fault latch event, the SWR Latch line transitions to the active low state. When in the normal high state, decoupling diode (D3) 1N914 is reverse biased, so no current flows through resistor (R7) 10 Kohms, so the behavior of Q1 is not altered when no SWR Latch fault is indicted. But when a protection trip instigated by excessive reflected power is detected, the low voltage on the cathode of diode (D3) causes resistor (R7) to conduct, pulling the base of transistor (Q1) low, shunting the output signal from Q2, thus removing the output bias to the optical isolator, effectively turning off the PWM modulator output when a fault occurs.

Frequency Selection:

The operator may select any transmit frequency within the 80 and 40 meter amateur phone band segments by rotating the frequency encoder knob. The LCD display will indicate the transmit frequency, in 1 KHz increments. The encoder is disabled during transmit mode, preventing a change in frequency until returning to receive mode. Although the encoder output is still received by the microcontroller input port pins, code in the microcontroller processing loop will disregard any input from these port pins when in transmit mode.

When transitioning between the 80 and 40 meter bands, the microcontroller automatically switches the appropriate bandpass filters into the RF output circuit, through a pair of SPDT relays, thus no band switch is required. It is interesting to note that these two relays will never be hot-switched, because the frequency may not be altered during transmit periods, thus a change in frequency between 40 and 80 meters can only occur when the transmitter is in standby, or receive mode.

The functionality of each of these processes is detailed in the Microcontroller Responsibilities, LCD Display Interface, Rotary Encoder, Band Switching Detection, and PLL VFO Generator Operation sections earlier in this document.

Tuning and Spotting:

The spotting switch is used to generate a carrier signal, without modulation, such that the transmitter may be set to match the frequency of the receiver, to join a net or ongoing QSO. If it is desired to start a new QSO, it is possible to simply set the transmitter to the desired frequency using the LCD frequency display readout; even in this case, spotting may be used to synchronize, or zero beat, the receiver to the transmitter frequency. Spotting is enabled by raising the front panel "SPOT" toggle switch.

Tuning:

Tuning, in this case, refers to placing the transmitter in transmit mode, albeit lower power (20 to 50 watts) in order to adjust such items as coupling networks or antenna tuners, so that a proper match is obtained before attempting to transmit at full power. Tuning mode is enabled by raising both the "SPOT" and "TRANSMIT" front panel toggle switches. The following paragraphs describe how the circuit accomplishes these functions:

First, it is beneficial to examine the operation while the "SPOT" switch is in the disabled, or down position. Transistor Q6, 2N2222, is forward biased by resistor (R31) 4.7 Kohms when the spot switch is ON, but with the spot switch OFF, this forward bias is shunted to ground, causing the emitter to collector terminals to appear as an open circuit. The collector is connected to the audio signal path, between the junction of (R30, C23) and audio coupling capacitor (C4). Thus, when spotting is OFF, the audio path is not interrupted, but when spotting is on, conducting transistor Q6 completely attenuates the audio signal, allowing a weak carrier signal to be generated, such that the receiver may be tuned.

Spotting:

When the "SPOT" switch is in the UP, or ON position, it enables two separate diode-decoupled circuits. First, Resistor (R) 10 Kohms, a pullup sourced by the 3.3 VDC supply, normally sets microcontroller input RC1 pin (12) to the high state, disabling the "SPOT" function. But with the switch on, Diode (D5), 1N914, between the pullup resistor and the spot switch, pulls the signal on microcontroller input RC1 to the low state, enabling the "SPOT" function.

Diode decoupling is necessary to allow the switch to perform more than one function, and to ensure the microcontroller is not exposed to voltages in excess of 3.3 VDC. The other function of the "SPOT" switch

is to pull down the 12 volt pullup provided by resistor (R10) 10Kohms, causing Diode (D4) 1N914 to conduct, pulling down the bottom of (R5) 27 Kohms, significantly reducing the positive bias applied to (Q2) 2N2222, supplied by resistor (R4) 10 Kohms, which sets the bias on Q2 base to control the output power generated by the PWM modulator section. This reduction in bias allows the transmitter to produce a lower level of output power when both the "SPOT" and "TRANSMIT" switches are both in the "ON" position. But, as was documented in the Transmit Receive Switching section, transmit power output is prevented when the "TRANSMIT" switch is off by the forward bias on (Q3) 2N2222, so the lower bias on (Q2) has no impact on the spotting function when not entering the "TUNE" mode.

In "SPOT" mode, the microcontroller enables the output of the PLL VFO chip (U4) SI570, by raising the signal on output port RC5 pin (16), pulling the Si570 enable pin (2) high to enable the PLL VFO output signal. Because the transmitter is NOT in transmit mode, the "TUNE" encoder is still enabled, allowing frequency mobility, and the PWM generator does not receive a bias to enable output, thus the class-D RF power amplifier stage is not enabled.

When adding the "TRANSMIT" enable switch to the above condition, "SPOT" continues to provide a reduced bias signal to control the PWM generator at low power output, without modulation, and the microcontroller enables the PLL VFO and 74HC74 flip flop, so the Class-D power amplifier receives the necessary RF drive and reduced DC supply voltages, producing the reduced power output required for tuning, before operating at the normal full output power.

IMPORTANT CAUTION!

If the transmitter experiences a protection trip while ether tuning or transmitting, BEFORE CYCLING POWER to reset the SWR Latch circuit, you MUST return both the transmit and spot switches to the down, (OFF) position. Turning on power with either of these switches enabled circumvents the normal power-up sequence, and will likely cause damage to circuits and components within the transmitter.

PLL VFO Generator Operation:

The Si570 Phase Locked Loop Variable Frequency Oscillator function is implemented by a Silicon Labs 10 MHz TO 1.4 GHz I2C Programmable XO/VCXO. This device produces a very stable, low level square wave.

The frequency is set as programmed by the microcontroller. In addition, the microcontroller may enable or disable the oscillator via a single control line, without the latency involved while addressing and transferring messages across the I2C bus.

The device is interfaced to the microcontroller via a two-wire I2C (Inter Integrated Circuit) bidirectional bus, and a separate, single bit port "output enable" signal. The I2C bus is an open-collector interface, comprised of one master controller and one or more slave devices, and requires external pull-ups, satisfied by (R24, R25) 10 Kohm resistors to the 3.3 VDC supply. Devices on the bus respond when polled by their unique addresses. Both master and slave devices may send and receive data on the bus.

The microcontroller is capable of functioning as an I2C master device, using port RC3 pin (14) for the clock signal connected to U4 SI570 pin (8), and port RC4 pin (15) for the data signal connected to U4 pin (7). This bus is used to initialize the PLL VFO mode, and set the PLL registers to produce the desired output frequency.

In this application, the output is four times the transmitter carrier frequency, divided by four by the 74HC74 flip flops, U5. Output is taken from the PLL VFO chip on pin (4). Note that the Si570 minimum output frequency is 10 MHz; in order to cover both the 80 and 40 meter amateur bands, the PLL output frequency must be divided. While dividing by a factor of four, it is possible to cover both bands without altering the 74HC74 division ratio when switching between these two bands.

Silicon Labs SI570

10 MHZ TO 1.4 GHZ I2C PROGRAMMABLE XO/VCXO

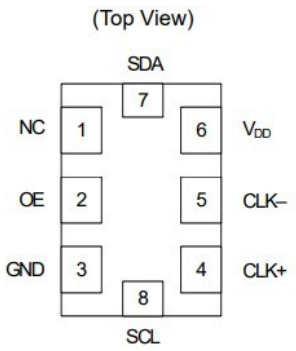


Table 13. Si570 Pin Descriptions

Pin	Name	Type	Function
1	NC	N/A	No Connect. Make no external connection to this pin.
2	OE	Input	Output Enable: See "7. Ordering Information" on page 24.
3	GND	Ground	Electrical and Case Ground.
4	CLK+	Output	Oscillator Output.
5	CLK– (NC for CMOS*)	Output (N/A for CMOS*)	Complementary Output. (NC for CMOS*).
6	V_{DD}	Power	Power Supply Voltage.
7	SDA	Bidirectional Open Drain	I^2C Serial Data.
8	SCL	Input	I^2C Serial Clock.
***Note:** CMOS output option only: make no external connection to this pin.			

SI570 Pinout and Pin Description Chart

SI570 PLL VFO: si570

https://www.mouser.com/catalog/specsheets/si570-571.pdf

74HC74 Frequency Divider Square Wave Generator:

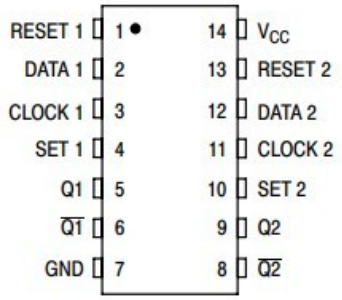
The low-level square wave output signal from the Si570 PLL VFO running with a 3.3 volt supply is used to clock both sections of a 74HC74 Dual D Flip Flop, U5, pins (3, 11). The 74HC74 is powered by U1 78L08 regulator providing 8 VDC. The resulting higher amplitude square wave output is one quarter the input frequency provided by the PLL VFO, and is now at the desired operating frequency. Output with the appropriate duty cycle is taken from flip flop 2 Q2 pin (9) and routed to the input of both IXYS IXDD614 gate drive ICs. This signal is interfaced via connector J5 pin (1) with pin (2) providing the ground return path.

Microcontroller output port RC6 pin (17) signal is routed to the reset input of both halves of the 74HC74 Dual D flip-flop, which may either enable or disable the pulse train sent to the gate drive integrated circuits.

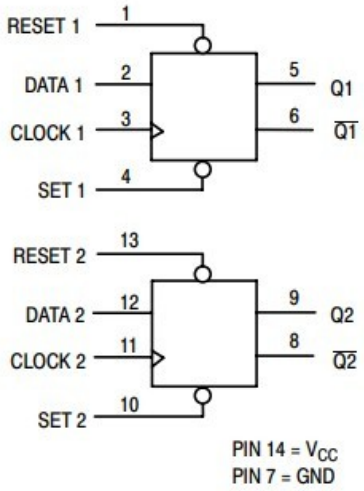
Texas Instruments 74HC74 Dual D Flip−Flop with Set and Reset

74HC74

PIN ASSIGNMENT



LOGIC DIAGRAM



FUNCTION TABLE

Inputs				Outputs	
Set	Reset	Clock	Data	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	No Change	
H	H	H	X	No Change	
H	H	↓	X	No Change	

Texas Instruments 74HC74 Pinout and Function Table

74HC74 Flip Flop: 74HC74

https://www.mouser.com/datasheet/2/308/74HC74-108792.pdf

Optical Isolator Function:

While the microcontroller and all the components on the front panel PCB operate using a power source referenced to chassis ground, the PWM generator and class-D final RF Amplifiers operate from floating high voltage supplies. The optical isolator is used to couple the audio and a DC bias to the PWM chip, thus enabling modulation and output power level control.

A CEL (California Eastern Laboratories) PS8602 PhotoCoupler U1 is utilized to isolate the source from the destination circuit. The LED in the optical isolator is driven by Q1 in the audio section of the front panel circuitry. in order to increase power level, a higher voltage is applied to the LED, and higher brilliance translates at the photoresistor to a larger drive potential to the internal output NPN transistor, configured in this application as an emitter follower. The audio signal rides on this bias level, alternating above and below the mean bias level.

This optical coupler is unique in that it provides an analog interface between the driver and the driven circuits. Most optical isolators operate in the digital, or binary mode, and transfer only the on-off, or zero-one status presented to the input light emitting diode. In this optical coupler, both the sending light emitting diode and the receiving photodiode operate in the analog realm, such that a DC bias applied to the LED, along with the analog audio signal, are faithfully transferred and processed by the output circuit photodiode and transistor, thus transferring an analog replica of the incoming signal to the isolated load circuit.

Input to the optical coupler is applied on U1 pin (3) with the ground return on pin (2). The U1 internal photodiode pin (8) and collector of the internal transistor, pin (6) are powered by the regulated + 5 VDC VREF output of the PWM generator chip, U2 pin (12). The regulated 5 VDC is filtered by (C15) .1 uF and (C1) 1 uF. The photodiode output is internally connected to the base of the transistor, and the output is taken from the emitter pin (5). Emitter follower output signal is developed across a series of resistors including (R19) 2.7 Kohms, variable resistor (R20) 1 Kohms, and (R8) 1 Kohms. Variable resistor (R20) is used to set the peak power limit. Output is taken across (R8), in parallel with (C4) .047 uF, and coupled to the VSCLAMP (Volt/Second Clamp) input of PWM generator U2 pin (9) via a series resistor (R7) 4.7 Kohms. The power level control bias and audio applied to this pin control the residual DC output level of the PWM circuit, and audio modulate the output via varying width pulses relative to the instantaneous audio amplitude signal.

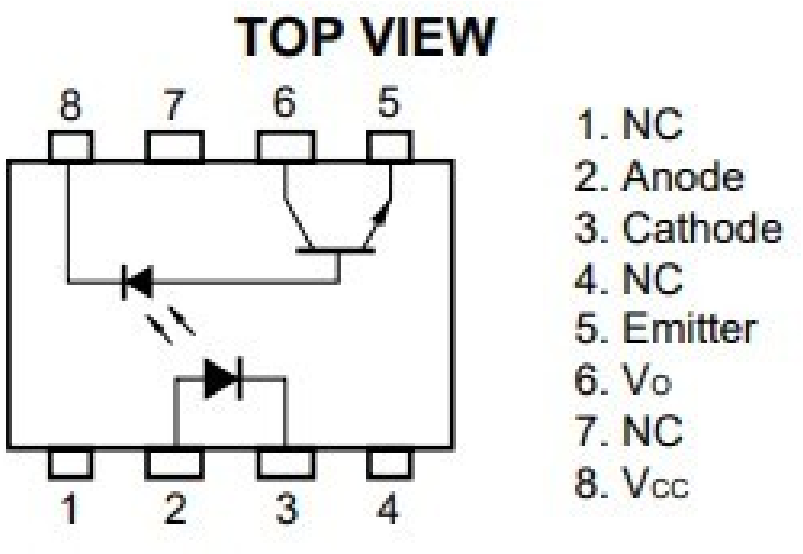
NEC may also manufacture a compatible substitute for the CEL component.

There has been a class problem symptom of transmitter power output increasing during longer transmissions as component temperatures rise. One confirmed fix for this issue is a replacement, or different version, substituted for the original manufacturer's Optical Isolator, also known as a PhotoCoupler. At the present time, the manufacturer or part number of the replacement that resolves the issue is not clearly defined. More current information regarding this subject may be available in the troubleshooting and repair document on the Wireless Girl website.

CEL California Eastern Laboratories

HIGH NOISE REDUCTION HIGH SPEED ANALOG OUTPUT TYPE 8 PIN PHOTOCOUPLER

The PS8602 and PS8602L are 8-pin high speed photocouplers containing a GaAIAs LED on input side and a P-N photodiode and a high speed amplifier transistor on output side on one chip. The PS8602 is in a plastic DIP (Dual Inline Package). The PS8601L is lead bending type (Gull wing) for surface mount.



USAGE CAUTIONS

1. This product is weak for static electricity by design, with high-speed integrated circuit so as to protect against static electricity when handling.

2. By-pass capacitor of more than 0.1 µF is used between VCC and GND near device. Also, ensure that the distance between the leads of the photocoupler and capacitor is no more than 10 mm.

3. Avoid storage at a high temperature and high humidity.

PS8602 Photocoupler: ps8602

https://www.mouser.com/catalog/specsheets/ps8602.pdf

PWM generator

Including Feed Forward Function, and "ILIM" Feedback:

PWM Basic Operational Overview:

A PWM Generator uses a comparator circuit to evaluate the relationship between the instantaneous output of a high frequency triangle wave generator and the audio modulation signal. As the comparator detects the sampled audio waveform at a higher amplitude than the triangle reference potential, the output rectangular signal is switched on, and when the modulation signal is less than the triangle reference level, the output rectangular signal is switched off. The net result is a switching (digital) output of a constant frequency, but with a varying width, or duration of each pulse, the duration of which varies in direct relationship with the instantaneous amplitude of the input audio voltage.

This digital signal is then amplified by switching output transistors, typically FETs, which operate at high efficiency, due to the fact that they are either cutoff (open circuit, no current flow) or saturated (maximum current, negligible source to drain resistance, resulting in extremely low device dissipation.

This high frequency, high voltage signal is then passed through a filter to remove the switching component, resulting in a highly amplified replica of the low-level input audio signal.

A bias is normally mixed with the input audio signal, setting the baseline pulse width, such that the output contains the DC potential necessary to provide the AM carrier, with or without modulation.

Either the positive or negative rail of the incoming DC may be switched, and in the case of this transmitter, the latter option was chosen.

Generator Chip Reference Information:

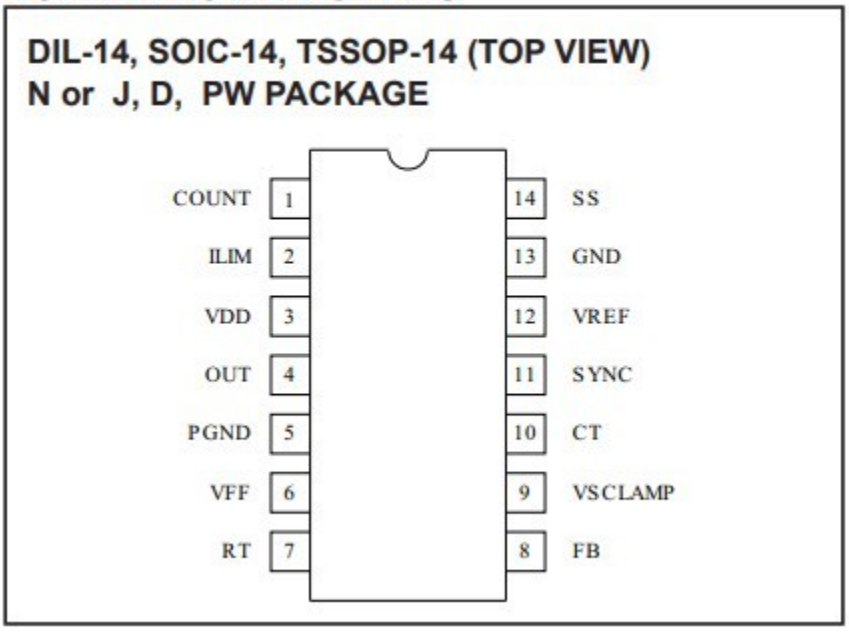
UCC15701 Advanced Voltage Mode Pulse Width Modulator

DESCRIPTION

The UCC35701/UCC35702 family of pulse width modulators is intended for isolated switching power supplies using primary side control. They can be used for both off-line applications and DC/DC converter designs such as in a distributed power system architecture or as a telecom power source. The devices feature low startup current, allowing for efficient off-line starting, yet have sufficient output drive to switch power MOSFETs in excess of 500kHz. Voltage feed forward compensation is operational over a 5:1 input range and provides fast and accurate response to input voltage changes over a 4:1 range. An accurate volt-second clamp and maximum duty cycle limit are also featured. Fault protection is provided by pulse by pulse current limiting as well as the ability to latch off after a programmable number of repetitive faults has occurred

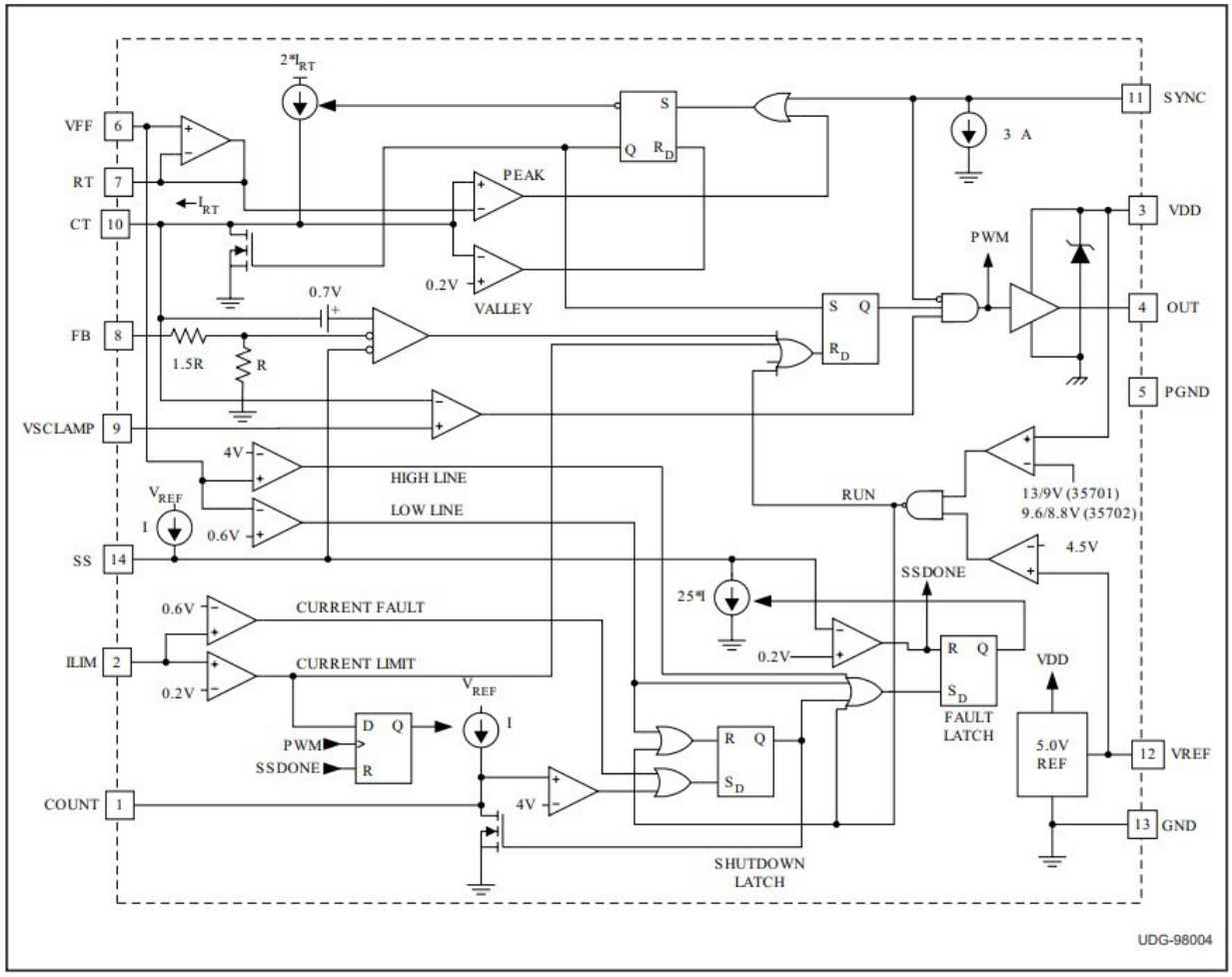
CONNECTION DIAGRAMS

DIL-14, SOIC-14, TSSOP-14 (TOP VIEW)
N or J, D, PW PACKAGE



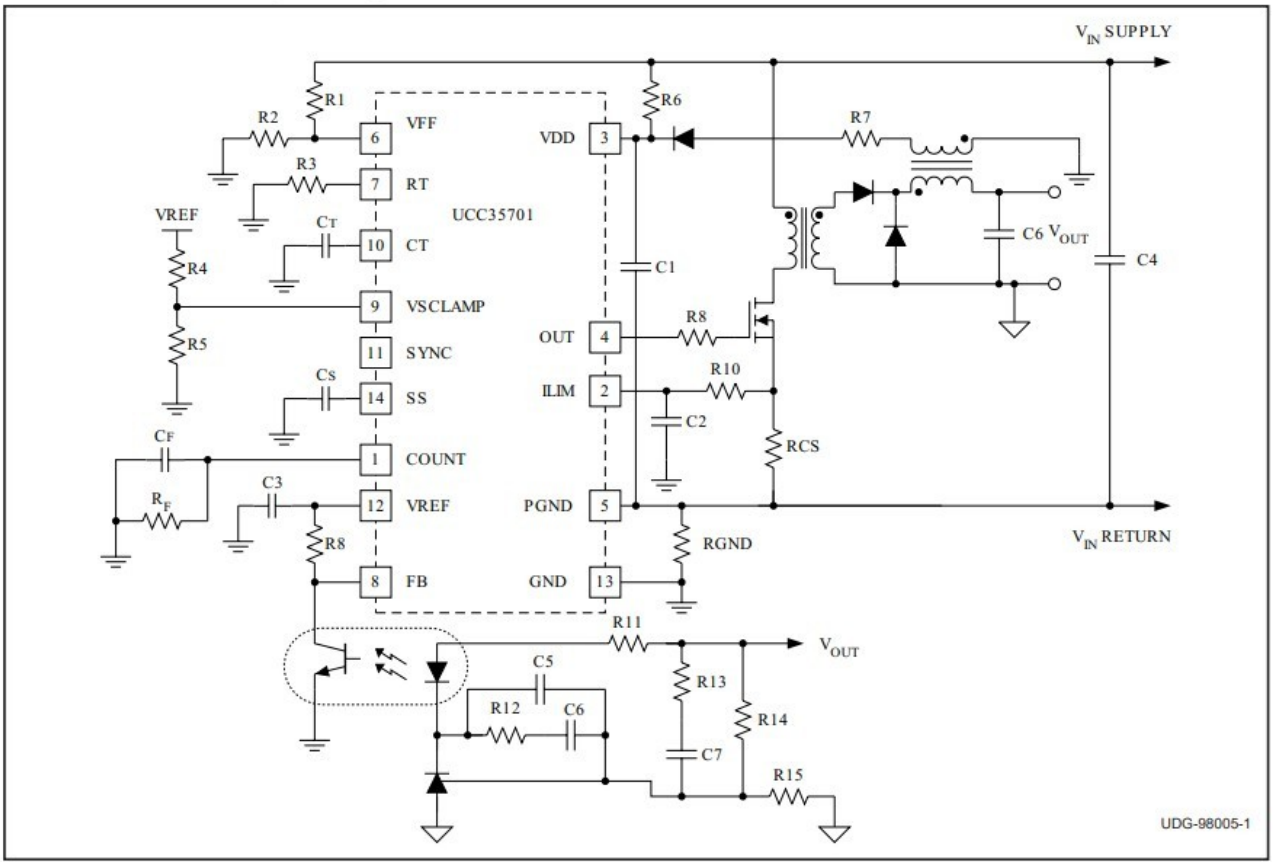
PWM Connection Diagram

DETAILED BLOCK DIAGRAM



PWM Generator Chip Detailed Block Diagram

TYPICAL APPLICATION DIAGRAM

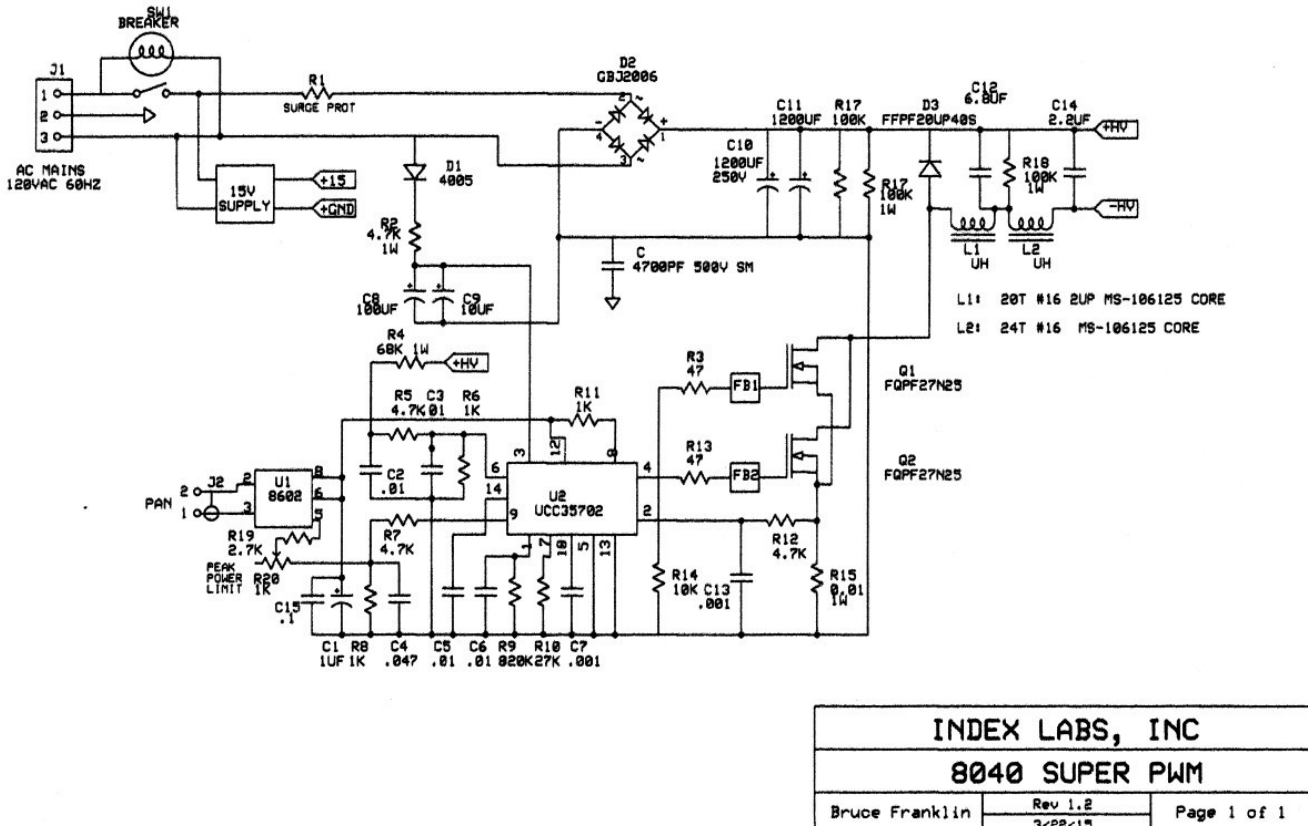


PWM Generator Chip Typical Application Diagram

For additional information defining the function and signal specifications for each pin, please refer to the manufacturer's detailed datasheet.

UCC1570X Voltage Mode Pulse Width Modulator: ucc35702

https://www.ti.com/lit/ds/symlink/ucc35702.pdf?ts=1774145062177



Schematic Diagram: K7DYY 8040 Super PWM

Power supply, PDM Generator and Modulator

PS8602 Photocoupler: ps8602

https://www.mouser.com/catalog/specsheets/ps8602.pdf

UCC1570X Voltage Mode Pulse Width Modulator: ucc35702

https://www.ti.com/lit/ds/symlink/ucc35702.pdf?ts=1774145062177

Specific DYY 8040 PWM Circuit Operation:

The PWM Generator employs a Unitrode Products (Texas Instruments) UCC35702 integrated circuit, commonly used as a PWM controller in switching power supply applications. When the UCC35702 is employed as an audio modulator for AM transmitters, instead of applying the varying output voltage to the feedback input to stabilize a regulated DC output voltage, the varying audio signal, with a bias to determine the desired DC output level, and therefore the final RF amplifier power output level, is used to control the PWM varying pulse width. By switching on and off, the power transistors (in this case, FETs) may operate in either cutoff or saturated states, greatly reducing dissipation and heat production, compared to typical analog amplifiers. This reduction in dissipation increases efficiency immensely. A filter network at the output removes the switching variations, but passes the full audio frequency range and DC power level, which then powers and modulates the final RF amplifier in a normal fashion.

The Floating High Voltage DC supply, described earlier, has its negative rail referenced to the PWM generator IC, coupling the generator output to the gates of two series switching FETs implemented in parallel. The varying negative output to the filter is taken from the FET drains; this negative rail, (after filtering), and the steady state positive output of the power supply, comprise the floating input power source to the RF amplifier section.

U2 power ground pin (5) and U2 signal ground pin (13) are directly connected to the negative rail of the power supply. DC power to U2 was described in the power supply section, but to reiterate, the DC positive potentials applied to VDD input pin (3), which employs an internal shunt regulator, limiting voltage to 14 volts at approximately 10 milliamperes. Feedback input is provided by a resistor (R11) from VREF pin (12) to FB pin (8).

Capacitor (C5) .01 uF determines the timing of the soft-start upon power on or when recovering from a fault, such as an over-voltage even, or an over current limit ILIM condition.

The frequency of operation is determined by the time constant of resistor (R10) 27 Kohms on terminal RT pin (7) and capacitor (C7) .001 uF on terminal CT pin (10). Normal clock frequency with this combination of components is expected to be in the vicinity of 75 KHz.

PWM output signal is taken from terminal OUT pin (4) and coupled to the switching FET gates via (R3, R13) and ferrite beads, equalizing gate drive and suppressing parasitic oscillations. There is a shunt resistor (R14) 10 Kohms from OUT to floating ground. A connection DOT is missing from the available schematic page of sheet 8040 Super PWM rev 1.2 dated 03/22/2015. The dot should be placed to the right of OUT pin (4) at the junction of (R3, R13, and R14).

In the 160/80 transmitter, there is only one PWM switching transistor of the same type as used in the RF section, whereas in the 80/40, there are two and these MOSFETs are lower Vdss transistors.

"ILIM" Feedback:

Output current limiting is managed by monitoring the voltage developed across current measurement shunt resistor (R15) 0.01 ohms, 1 watt. Network (R12) 4.7 Kohms and (C13) .001 uF condition and filter the pulses, providing an average current measurement value to the PDM generator input ILIM (current limit) on pin (2).

Capacitor (C6) ,01 uF and Resistor (r9) 820 Kohms connected between floating ground and the COUNT terminal pin (1) define the behavior and response to the current measurement feedback applied to ILIM pin (2).

Feed Forward

A feature known as "Feed Forward" is often employed in switching power supplies, and is also applicable to the PWM modulator implementation. In essence, it is another feedback loop, which monitors both the dynamic stability and the noise and ripple at the filter capacitor output of the high voltage supply. This feedback acts to reduce output noise and ripple, while improving dynamic regulation, allowing somewhat smaller filter capacitors to be used than would be required without this form of feedback.

This feature is implemented by attenuator resistor (R4) 68 Kohms sampling the positive high voltage supply rail; the error signal is conditioned by network (C2, C3) each .01 uF, and (R5) 4.7 Kohm, (R6) 1 Kohm, applying the conditioned error signal to the VFF (Voltage Feed Forward) input pin (6) of the PWM generator IC.

PWM Filter Network and Components:

The current switched by the FETs is passed from the FET drains to the PWM output filter network, consisting of inductors (L1, L2) and capacitors (C12) 6.8 uF, (C14) 2.2uF, and on sheet 8040 Super RF, (C5, C6), each .15 uF. (The modulated DC input capacitors in the RF amplifier section are in parallel with the PWM filter output capacitor (C14) and therefore must be included in the filter design and tuning calculations.) The output filter must be carefully tuned to the PWM switching frequency, as determined by RT and CT resistor and capacitor, (75 KHz), as described previously.

Damper diode (D3) is a fast-acting high-current device, responsible for conducting when the output FETs transition from conducting mode to open-circuit mode, such that stored energy in the PWM filter inductors is safely dumped back into the power supply filter capacitors instead of being allowed to rise to levels that would damage the output switching FETs.

IXYS IXDD614 FET Gate Drivers:

In driving transistors for switch-mode transmitters, we would prefer the base or gate to be driven by a pure, unmodified square wave in order to develop the greatest power efficiency during switching. However, due to the relatively large parasitic capacitance of the base or gate nodes (for mosfets it denoted as Ciss), the actual waveform seen at the gate or base is not a pure square wave pulse but is modified. This base or gate capacitance also presents a low impedance to the driver at high frequencies. Low impedance drivers with a series resistor may be used. Here, low-impedance-transformation-ratio gate drive transformers are used.

The K7DYY gate drive circuit consists of the IXDD614 gate driver, a series inductor, a series DC blocking/coupling capacitor, and a dual secondary drive transformer. The secondaries are effectively across the Source-Gate nodes. The driver is powered by 19 volts so that a large voltage amplitude is available for sufficient current drive in the 40 meter mode. The small-valued L, the L of the transformer primary, along with the coupling capacitor, constitutes a wideband sawtooth waveform circuit. The drive transformer secondaries are resistively loaded for frequency broadening and to limit the gate voltages in the 80-meter mode. As per the literature, a sawtooth is the preferred gate drive waveform.

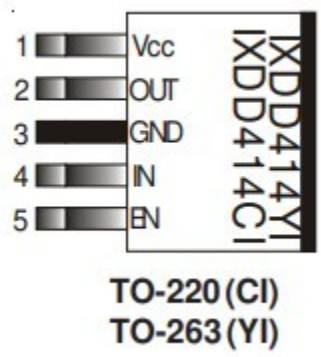
The substitution of different mosfets with different Ciss specifications should be approached with caution because this may affect the drive requirements and the shape of the gate node waveform. For example, a device with a lower Ciss may allow increased ringing on the secondary of a gate drive transformer unless that transformer has increased resistive loading.

Historically, it appears that the earlier IXDD414 component was initially used in the 80/160 Super Senior, but when the 414 was obsoleted, replaced by the IXDD614, the newer component was employed in both the 80/160 and the 80/40 products. Each device is available in two variants, a four-pin device with no enable control line, and a five pin component which includes an enable line. The Super Senior transmitters employ the five pin device, however the enable pin is permanently tied high to the positive device supply rail.

Scoping the waveforms at the gate nodes is the only way to determine device compatibilities.

SYMBOL	FUNCTION	DESCRIPTION
VCC	Supply Voltage	Positive power-supply voltage input. This pin provides power to the entire chip. The range for this voltage is from 4.5V to 25V.
IN	Input	Input signal-TTL or CMOS compatible.
EN	Enable	The system enable pin. This pin, when driven low, disables the chip, forcing high impedance state to the output.
OUT	Output	Driver Output. For application purposes, this pin is connected, through a resistor, to Gate of a MOSFET/IGBT.
GND	Ground	The system ground pin. Internally connected to all circuitry, this pin provides ground reference for the entire chip. This pin should be connected to a low noise analog ground plane for optimum performance.

IXDD414 and IXD614 Pin Description



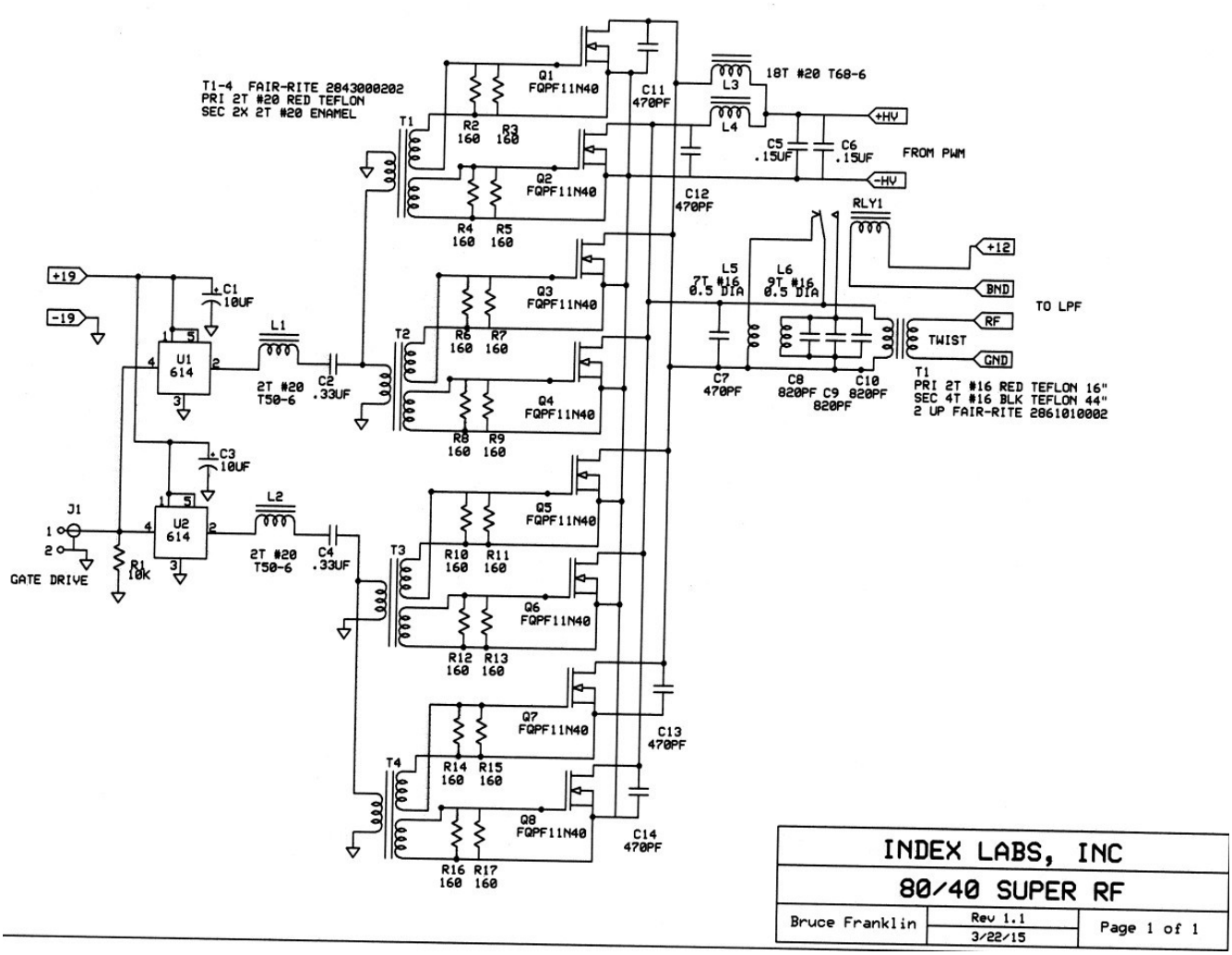
IXDD414 and IXD614 Pinout for TO-220 package

Ultrafast MOSFET Driver IXYS XDD414P1

https://www.mouser.com/datasheet/2/240/99061-1546545.pdf

Current Mode Class-D RF Amplifier:

The RF Amplifier section of the transmitter is presented on page "8040 Super RF" in schematic the diagram file. The implementation is based upon the highly-efficient Current Mode Class-D amplifier technology. In order to achieve the desired power level, four pairs of power FET transistors are arranged with their outputs in parallel, however each FET employs a dedicated gate drive circuit, as described in a previous section.



Schematic Diagram: K7DYY 8040 Super RF

Gate Drivers and RF Amplifier

The basic architecture for a CMCD power amplifier consists of a pair of FETs in switch mode, each driven alternately to saturation or cutoff, with the current source supplied from VCC to each FET drain through a separate RF choke. A resonant tank circuit is connected between the drains of the alternately conducting FETs, the output transformer coupled with the primary in parallel with the tank circuit.

Both transistors operate as switches driven by a square wave 180 degrees out-of-phase. The gate drive waveform is critical to ensure that both transistors never conduct simultaneously. The current

flowing in the load network is a square waveform with null DC value. Ideally, there are no voltage harmonics besides the fundamental frequency, because the LC filter short-circuits the resistive load for any frequency other than the fundamental one. As a result, the differential voltage taken at the drains of the transistors is a sinusoidal waveform.

Ideally, the switches only have voltage across them or current flowing through, never both. This non-overlapping feature of voltage and current enables the current mode class-D amplifier to run at maximum efficiency.

Referring to the 8040 schematic diagram, note that all even-numbered FETs have their source and drain connected in parallel. Likewise, all odd-numbered FETs are also parallel-connected. Thus, the circuit may be studied by focusing on Q1 and Q2, ignoring the other paralleled devices, assuming every FET in each pair receives appropriate gate drive. NOTE: An error in the8040 Super RF schematic diagram is missing a connector “dot” connecting the source of FET Q7 to the vertical common source bus between Q7 and C13. RF choke (L3) provides positive source supply VCC to Q1, and (L4) likewise supplies Q2. The resonant tank network for 40 meters consists of capacitor (C7) 470 pF in parallel with inductor (L5). When relay RLY1 not energized (in the normally closed state), the 40 meter resonant tank is connected in parallel with the drains of Q1 and Q2, and the output is coupled by T1, with the primary connected in parallel with the tank circuit. When switching to 80 meters, relay RLY1 is energized, disconnecting 40 meter (L5), and connecting 80 meter inductor (L6), as well as additional parallel capacitors (C8, C9, and C10), each 820 pF.

The digital drive generated by the PLL VFO SI570, divided by the 74H74, is set to the correct frequency by the microcontroller, and no other changes to the input drive network are required to accomplish the switch between the 40 and 80 meter bands.

Shunt capacitors (C11, C12, C13, and C14) each 470 pF, in parallel with the various FETs from source to drain, serve two functions. When the FETs switch from the conducting state to the open circuit state, the capacitors serve to limit the high voltage turn-off spikes, protecting the FETs. They also are part of the capacitance comprising the output tank circuit. If these capacitors are too small, transients are not sufficiently quenched. If they are too large, switching is damped, and overall efficiency suffers.

Substituting different mosfets with a different Coss will have a cumulative effect on the overall drain to drain capacity (between the parallel FETs on alternate side of the push pull output circuit. This change may require adjustments to the overall total value of the snubbing capacitors (C11 - C14), and will also affect the resonant output tank resonant frequency. These different components may also require adjustments to the cumulative value of the parallel tank capacitors, inductors, or both, to maintain resonance, desired tank circuit Q, and overall efficiency.

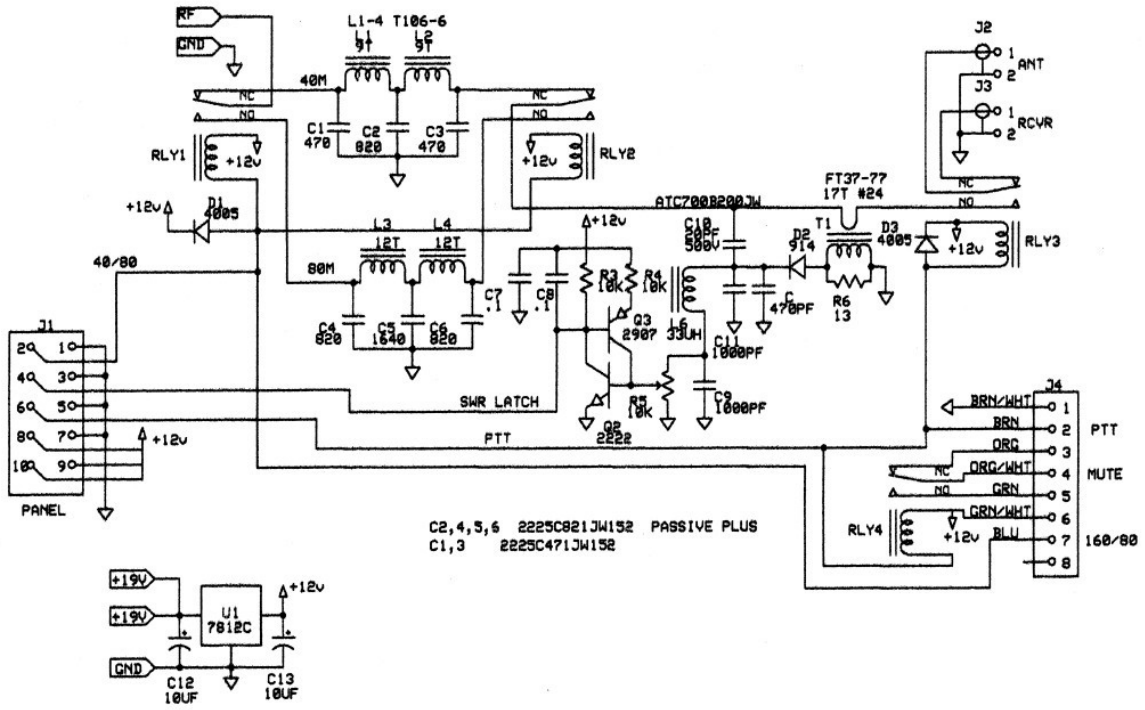
As referenced earlier, the additional parallel FETs increase the overall power capability of the amplifier. Output is taken from the secondary of the transformer T1, and passed to the low pass filter circuits described on sheet 8040 Super LPF.

Modulated high voltage is supplied to the Class-D amplifier section from the line-sourced bridge rectifier and filter capacitors in the power supply section; the negative rail is modulated by the PWM Modulator output switching FETs, and filtered by the four-pole LC PWM filter network. As a result, the positive supply rail is at a constant DC potential, while the negative supply rail fluctuates up and down with modulation. Due to the floating power supply implementation, it is necessary to isolate the gate drive and RF output power from associated chassis-ground-referenced circuits. This requirement is satisfied in two ways: by the galvanic isolation of the individual gate drive transformer secondary windings for each of the eight individual FETs, and the output coupling transformer T1, transferring the generated RF energy to the appropriate low pass filter as documented on sheet 8040 Super LPF. The other isolation method for audio coupling is accomplished by the photocoupler U1.

Butterworth Low Pass Filter Networks:

The broadband tank circuit within the Class D RF amplifier does not provide sufficient harmonic and spurious suppression, therefore the RF output transformer is coupled to a separate Butterworth low pass filter for each band.

Illustrated on 8040 Super LPF schematic sheet, each low pass filter is implemented with two Pi, or Pi L networks in cascade. The 40 meter filter consists of (L1, L2, C1, C2, and C3). The 80 meter filter employs (L3, L4, C4, C5, and C6). These low pass filters include no adjustable components for tuning, and are designed to work into a matched impedance of 50+j0 ohms; any significant mismatch results in a rather excessive levels of SWR, and the resulting reflected power will inhibit normal operation.



INDEX LABS, INC		
8040 SUPER LPF		
Bruce Franklin	Rev 1.0 8/20/14	Page 1 of 1

Schematic Diagram: K7DYY 8040 Super LPF

Low Pass Filter, SWR Protection

Relays RLY1 and RLY2 connect the input and output of the 40 and 80 meter filters, respectively. When not energized, the normally closed contacts enable the 40 meter filter; when energized, the normally open contacts enable 80 meter operation.

The relay coils, in parallel, are tied to +12 volts, and the "BAND' control signal from the front panel circuit, where switching transistor Q4 (BCP68) conducts to close the relays when an 80 meter frequency is dialed in with the TUNE knob. Also in parallel with these relays is a third relay, RLY1 on the 8040 Super RF schematic, which selects the proper tank circuit components for the band in question.

Diode (D1) 1N4005 is in parallel with relay (RLY1), and is reverse-biased when the relay is energized. When the relay is de-energized, the diode conducts and snubs the counter-emf energy stored in the relay coil, thus preventing damage to the switching transistor. Because the other two relays are in parallel with (RLY1), a single diode provides protection from stored energy in all the relay coils.

Two additional relays perform the functions needed to transition between receive and transmit mode. RLY3 switches the antenna connector between the receiver connector via normally closed contacts (relay de-energized), and the low pass filter output (normally open contacts (relay energized). In parallel with the coil for (RLY3) is the coil for (RLY4), an assessor labeled as MUTE, intended to silence the receiver while in transmit mode. This relay provides normally closed, common, and normally open terminals accessible vi accessory jack J4, pins 3, 4, and 5 respectively. This combination of contacts should allow muting of virtually any receiver. The contacts may also be used for any other control function, within the contact voltage and current rating. Like the band switching relays, a snubbing diode (D3) 1N4005 (for both relays in parallel) is placed in parallel with RLY3 coil, to protect the circuitry connected to the PTT control line.

The sole source for Transmit/Receive transition control is the + 12 volt supply tied to one terminal of each relay. This signal is used by other circuits on the front panel PC board, and it is HIGH (+12 volts) during receive periods, and LOW (0 volts) during transmit periods. (While this +12 volt signal appears on the PTT bus during receive mode, it may be used by high impedance loads for any desired logic switching, for example, level shifting to the +3.3 VDC via the diode and pull-up resistor signal to the PIC pin 7 discussed earlier, but it must not be used to source any significant current, as it would then attempt to close the transmit receive relays described above).

Transition from receive to transmit mode may be invoked in several manners:

1) closing the transmit toggle switch on the front panel,

2) pressing the push-to-talk switch on a microphone, grounding microphone connector pin (4),

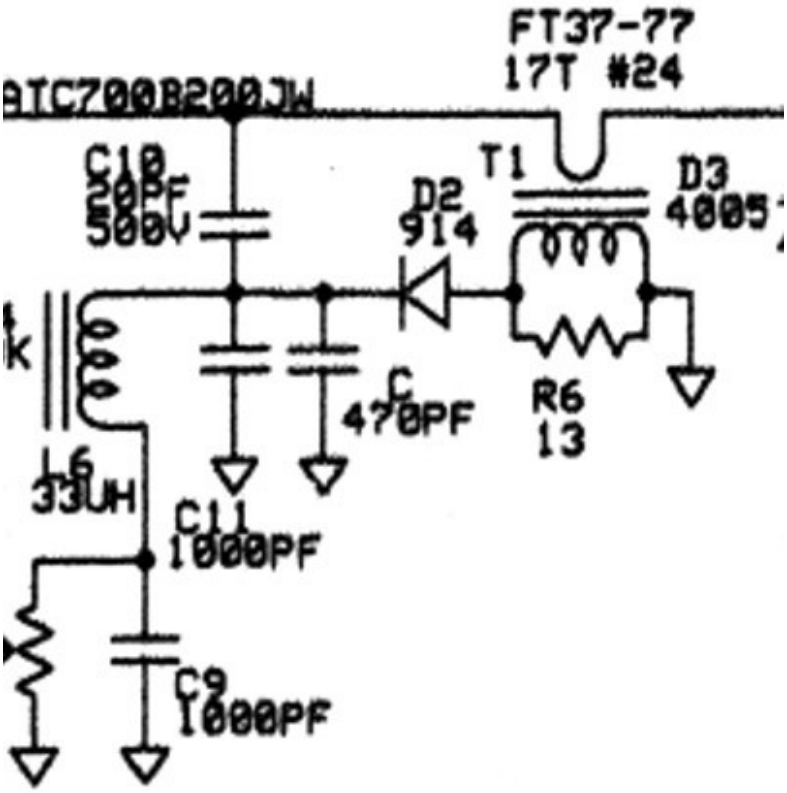
3) grounding accessory jack J4 pin (2).

In addition to the MUTE and PTT signals available on connector J4, other circuits available are ground, +12 volts DC, and 40/80 band select on pins (1, 6, and 7), respectively.

There is no connection to pin (8).

Reflected Power Detection:

To protect the transmitter circuits from excessive SWR resulting from a load mismatch, a reflected power sensing circuit is included. The output RF signal from the low pass filter to the transmit receive relay is passed through a transformer core, T1. Current is detected by the transformer, and voltage is detected by (C10) 20 pF 500 volt ATC multi-layer ceramic capacitor. These, in association with diode (D2) 1N914, (C) 470 pF, and (C11) 1000 pF sample and rectify the reflected power, the resulting voltage is then filtered by (L36) 33 uH and (C9) 1000 pF, and applied to variable resistor (R5) 10 Kohms. The adjustable output from this resistor is utilized to determine when the reflected power level has reached a dangerous level, allowing the Protection Trip Logic to take preventive action.

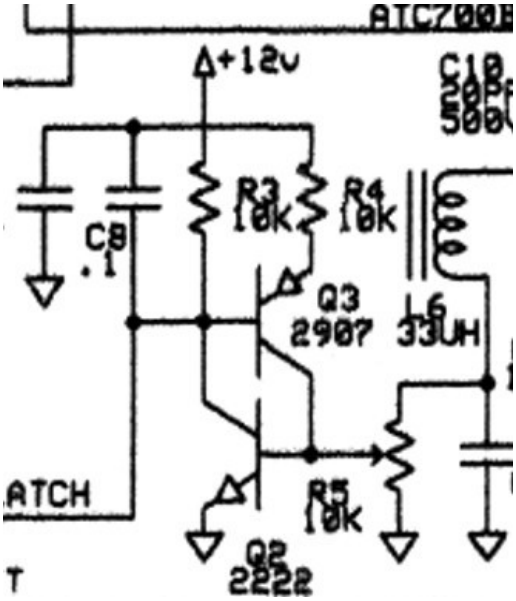


SWR Reflected Power Sense Circuit (Output to SWR Latch Circuit)

Protection Trip Logic:

Variable resistor (R5) is adjusted at the factory to provide the correct level of sampled reflected power such that a latch circuit employing Q2 and Q3 may provide a negative-logic BINARY LATCH when an excessive reflected power situation occurs. This adjustment is intended to enable the latch circuit to explicitly shut down the PWM generator AND the RF Drive Pulse Train in the event the level is sufficient to trip the latch. Once latched, the two transistors maintain the latch status until the +12 volt supply is removed by switching off the main power switch/breaker.

The processor and other circuits on the front panel circuit board receive this binary signal, and have no involvement in the decision of when to latch, or at what level to latch. While the input pin on the PIC may be programmed to function as either an analog or digital port, a finite decision is made by the latch circuit on the low pass filter board, and the PIC microcontroller simply responds to the digital signal provided by the latch.



SWR Latch Circuit (Input from SWR Reflected Power Sense Circuit)

Latch operation functions as follows:

Transistors (Q2) 2N2222 and (Q3) 2N2907 are cross-coupled, such that the collector output of Q2 is tied to the base of Q3, and the collector of Q3 is tied to the base of Q2.

Initially, the base of Q2 connected to the variable wiper of potentiometer (R5) is at ground potential, equal to the emitter potential, so the transistor does not conduct when no SWR DC signal is present. The base of Q3 is tied to +12 VDC, at the same potential as its emitter, tied to +12 VDC by (R4) 10 Kohm. Therefore, in the normal state, neither transistor conducts.

When SWR reflected power becomes excessive, the setting of R5 is such that the forward bias on the base of R5 causes sufficient current through collector resistor R3 to cause Q3 to conduct. This in turn causes current through Q3 emitter current to increase, thus increasing the forward bias on the base of Q2. Momentarily, this action causes both transistors to go into saturation, and this status persists until the + 12 volt supply is removed from (R3) and (R4). Due to Q2 being in saturation mode, very little voltage appears between the emitter and collector; thus almost all of the 12 volt supply is dropped across collector resistor (R3). This pulls the SWR latch from the normal HIGH state to a LOCKED, or LATCHED LOW state. The SWR LATCH status is passed to the front panel PCB via J1 pin (4). This circuit action reveals conclusively that the determination of the SWR protection trip is made solely on the Low Pass Filter board, and the PIC simply follows the command and disables the PLL VFO and digital drive to the Class D RF amplifier. Separately, on the front panel board, as discussed earlier, the SWR Latch is also coupled via Front Panel diode (D3), and via resistor (R7), the bias on Q1 is quenched, thus disabling the PWM input, removing the modulated DC supply potential from the RF power amplifier circuit.

Bibliography:

Original manufacturer datasheet content links are listed below.

Manually browse to review the relevant data as desired.

Data sheets may not be stored on the web server due to copyright restrictions.

16F872 Microchip "PIC" Microcontroller: 30221cPIC:

https://ww1.microchip.com/downloads/en/DeviceDoc/30221c.pdf

Liquid Crystal Data Display: NHD-0108CZ:

https://newhavendisplay.com/content/specs/NHD-0108CZ-FL-GBW.pdf

SI570 PLL VFO: si570:

(https://www.mouser.com/catalog/specsheets/si570-571.pdf

74HC74 Flip Flop: 74HC74:

https://www.mouser.com/datasheet/2/308/74HC74-108792.pdf

Ultrafast MOSFET Driver IXYS XDD414P1:

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PS8602 Photocoupler: ps8602:

https://www.mouser.com/catalog/specsheets/ps8602.pdf

UCC1570X Voltage Mode Pulse Width Modulator: ucc35702:

(https://www.ti.com/lit/ds/symlink/ucc35702.pdf?ts=1774145062177)

CTS Model 636 HCMOS Clock Oscillator: clock-ocillators-636-datasheet:

(https://www.ctscorp.com/Files/DataSheets/Passives/FCP/Clock-Oscillators/clock-ocillators-636-datasheet.pdf)

And that is all I have to say about that

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